2133

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In re the application of
Lee D. Whetsel TI-30726

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Title: Adapting Scan BIST Architecture for Low Power Operation

Information Disclosure Statement A

February 20, 2004

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
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Lawrence J. Bassuk, Reg. No. 29,043

Dear Sir:

Applicant requests consideration of all US patents, foreign patents and other documents listed on enclosed form PTO-1449, and includes a legible copy of only those documents listed under the foreign patent and other document headings.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Applicant points out particular references and figure numbers and provides a brief explanation of each cited reference in Attachment A. Please also see the following patents:

US 5,150,044 Hashizume

US 6,519,729 Whetsel

Please consider this statement as being filed under Rule 97(c), after the period specified in Rule 97(b), but before the mailing date of either a final action, or a notice of allowance. Under Rule 97(c), applicant submits the fee set forth in Rule 17(p). Please charge the fee under Rule 17(p) of $180.00 to Deposit Account Number 20-0668 of Texas Instruments Incorporated. We enclose two copies of this sheet.

Respectfully submitted,

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Attachment A

In the following, a brief description may contain a statement that the patent corresponds to one or more other patents. No description of the corresponding patents is provided to avoid duplicating a description of the same disclosure.

The described patent may be a divisional of or a continuation-in-part of the corresponding patent. A corresponding patent may be a divisional of the described patent. A corresponding patent may have issued from one of plural applications that appear to have the same drawing figures and were filed on the same day as the described patent. A corresponding patent may be a foreign patent claiming priority from the described patent or it may be a foreign patent providing priority for the described patent.

US Patent Documents

Re. 31,056 to Chau et al. discloses a high speed testing circuit 10 coupled between a test system computer 12 and a device under test 14. The circuit 10 supplies stimuli signals, receives output signals, and provides parametric testing. Reissue of US 4,092,589.

US 3,633,100 to Heilweil, et al., discloses applying two binary levels and an intermediate level of inputs to binary logic under test and to simulation logic. The outputs of the circuit under test and the simulation logic are compared to ascertain a good circuit

US 3,651,315 to Collins discloses a digital inspection system. The outputs from a product under test are compared with the outputs of a known good unit.

US 3,657,527 to Kassabgi, et al., discloses a system for automatically checking boards bearing integrated circuits. A program card is read automatically to provide both test input signals to the board and simulation output signals representative of the correct output signals.

US 3,723,868 to Foster discloses digitally counting predetermined numbers of clock pulses during preselected timing intervals to determine the precise time interval between distinct edges of the output from a circuit under test and provide a GO/NO-GO indication.

US 3,739,193 to Pryor discloses a feedback network where the feedback signal is sufficiently small to be overridden by the input signal.

US 3,789,359 to Clark, Jr., et al. discloses a synchronism indicator for a convolutional decoder.

US 3,824,678 to Harris, et al. discloses a process for laser scribing beam lead semiconductor wafers.

US 3,826,909 to Ivashin discloses a binary counter applying identical signals to a tested and standard reference circuit. Output indicators display any difference between the tested and standard reference circuit.

US 3,831,149 to Job discloses a control device having presettable control elements, one for each test lead, each presettable to a desired state for specifying signal-combinations to be monitored. The signal-combinations control the read-in and/or read-out of information from a memory.

US 3,838,264 to Maker discloses a device for checking the contents of a store of a computer that is normally under control of a chain of timing pulses and an address register. The device

includes a switching device that sums a quantity of the timing pulses and compares the sum to a known quantity.

US 3,873,818 to Barnard discloses reducing the size of a random access memory storing test patterns. Similar test words are stored as an initial word with indications and binary reconstruction means for generating the other similar test words.

US 3,976,940 to Chau et al. discloses a test circuit 10 including a pair of comparator circuits, each of which is disposed for comparing two minimum threshold amplitudes of responses from a device under test. A multiplexer switches the outputs of the two multiplexers to the device under test.

US 4,023,142 to Woessner discloses a common reliability and service bus connected to each functional unit of LSI apparatus. The bus provides for an addressed unit to go through an operation after a test pattern has been loaded into the unit while the system continues to operate concurrently. Figure 4 depicts a control system adapter 200 with shift register configuration 210. Data bits 0-7 appear to be loaded in parallel into Diagnostic Address Register 175, Mode Register 1 120, Mode Register 2 180, Mode Register 3 185, and Shift Register 170. Level Shifting Serial Design latches 210 form a scan path. An exclusive OR circuit 400 compares the data from shift register 210 to be compared serially, bit-by-bit, with an expected data pattern loaded into register 170.

US 4,066,882 to Esposito discloses an automatic computer controlled digital test device that tests circuits by other than random test techniques. The device relies upon software test generation techniques and test programs written in high level test languages and stored on a magnetic disk.

US 4,086,375 to LaChapelle, Jr., et al. discloses a batch process providing beam leads for microelectronic devices having metallized contact pads.

US 4,092,733 to Coontz, et al. discloses an electrically alterable, non-volatile interconnect that selectively connects and disconnects microcircuit elements formed on a wafer. Corresponds to JP 52-136,534.

US 4,108,359 to Proto discloses a device for detecting errors in the execution of a sequence of coded instructions. A feed-back shift register generates a digital sequence combined with the sequence of instructions to compute a unique sequence check word that is compared to a stored, known good check word.

US 4,146,835 to Chnapko et al. discloses a method of testing the difference in propagation delays through gate circuits of an integrated circuit. The method generates a reference signal at the sensing of the first output of one of the gate circuits and adding a maximum delay time. Any actual signal occurring after the end of the maximum delay time indicates a delay beyond specification.

US 4,161,276 to Sacher, et al. discloses comparing transitions and final logical states of a known good part with a part under test.

US 4,216,539 to Raymond, et al. discloses a programmed processor controlling a set of switches to apply a test signal to a selected node and connect the response from that node to a functional tester.

US 4,242,751 to Henckels, et al. discloses peripherally probing circuit boards and the like with insights into predictable or likely failures and over-riding or discontinuing normal computer back-tracking.

US 4,264,807 to Moen, et al. discloses an electric counter including a pair of counter segments connected in cascade. The counters count in Gray code. The second counter segment

increments upon the first segment changing from 10 to 00. Corresponds to EP 0,017,091 and JP 55-135,424.

US 4,268,902 to Berglund, et al. discloses a maintenance interface for interfacing a service processor and a central processor operating synchronously to each other. The interface circuitry synchronizes the service processor to the central processing unit and decodes commands from the service processor. The interface circuitry also establishes communication from the central processing unit to the service processor and resolves communication contention between the processors.

Circuitry provides independent control of the clocks to each functional unit or shift ring (scan path) and the functional unit interface signals to other functional units or arrays. The interface includes a Level Sensitive Scan Design (LSSD) testing system with four separate shift rings and provides degating of central processing unit interfaces as required for this testing approach.

US 4,286,173 to Oka, et al. discloses a logical circuit having bypass for testing logical circuits. Corresponds to JP 54-127,245.

US 4,308,616 to Timoc discloses simulating a fault on a selected connection with the output of a shift register in a digital network.

US 4,309,767 to Andow, et al. discloses a monitor system judging the operating condition of an A-D converter from the contents of an adder.

US 4,312,066 to Bantz, et al. discloses an interface between a host processor and a diagnostic/debugging processor that troubleshoots the hardware and software of the host processor. The host uses the Level Sensitive Scan Design rules.

The disclosed system allows the machine state and memory of the Host CPU to be captured at the end of an instruction or at the end of a cycle. It further allows selective reading and writing of the memory state by conditioning the H-machine with state information that will cause words from or to memory to be transferred to the D-machine. The system allows control over interruption, channel activity and address translation and provides a diagnostic CPU with its own memory to perform diagnostic and debug functions.

US 4,339,710 to Hapke discloses a MOS integrated circuit using field effect transistors including a circuit arrangement for rapidly testing various blocks of the circuit.

US 4,357,703 to Van Brunt discloses performing dynamic testing of complex logic modules at full system clock rates and is resident on each LSI chip under test. The test system includes transmission gates to alter logic paths, and an associated test generator and accumulator at each of the test input and test output.

US 4,365,334 to Smith, et al. discloses producing final test data in response to a stored Logic List for each logic circuit type and stored connection information for a logic circuit under test.

US 4,366,478 to Masuda, et al. discloses a general purpose signal transmitting and receiving apparatus for transmitting and receiving signals between a bilateral bus line and a serial-by-word data transmission line.

US 4,390,969 to Hayes discloses an asynchronous data transmission system with state variable memory and handshaking protocol circuits. The circuit is a stored state circuit including a memory and an output register with an input line and an input request line coupled to the memory and the output register having an output data line and an output acknowledge line.

US 4,426,697 to Petersen, et al. discloses a bus systems with address and status conductors. The address conductor carries mutually spaced serially binary coded bit patterns of m address bits, and the status conductor carries a serial bit pattern or r status bits.

US 4,433,413 to Fasang discloses a microprocessor system including a pseudo-random pattern generator, a signature register, supplemental control logic, serial and parallel I/O port test logic, and an LED display. Test instructions and the pattern generator provide test input data. The signature register and the microprocessor process the test results and present them on the display.

US 4,439,858 to Petersen discloses a digital in-circuit tester for high speed computer control in obtaining high pulse fidelity at each electrical node of a circuit under test. The tester includes a plurality of programmed memory digital test-signal generators responsive to the computer for generating and supplying to the nodes of the circuit under test a complex sequence of digital logic signals. High pulse fidelity is obtained by minimizing the current in the power supply and digital test signal loops.

US 4,441,075 to McMahon discloses the testing of individual chips and interchip connections on or within a high density packaging structure without a precision probe using Level Sensitive Scan Design rules. Basis for divisional patents US 4,494,066 and US 4,504,784.

US 4,483,002 to Groom, Jr., et al. discloses defining a display window for display of signals at selected test points. An operator defines signals at the beginning of the window and at the end of the window, but only after specified conditions. Corresponds to EP 0,093,229 and JP 58-190,784.

US 4,484,329 to Slamka, et al. discloses the jaw contacts of a clip 10 connecting a device under test to the external interface block 14 of a test device. Signals from the device under test are compared with signals output from a library block 20.

US 4,488,259 to Mercy discloses Level Sensitive Scan Design strings on an integrated digital logic circuit to provide multiple functions of providing control parameters to logic blocks in the integrated circuit chip, and for providing reconfiguration messages to reconfiguration logic on the integrated circuit chip, in addition to the normal function of transferring test data to various portions of the integrated circuit chip. This reduces the number of input/output pads on the integrated circuit chip which must be dedicated to these functions.

US 4,493,077 to Agrawal et al. discloses LSI circuits including level sensitive mater latches and slave latches receiving two clock or control signals for normal mode operation. The conditions to initiate the scan testing mode are imposed on the standard clock terminals.

US 4,494,066 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level sensitive scan design rules need to be used for each chip and for the package clock distribution network. Divisional patent of US 4,441,075 and corresponds to US 4,504,784.

US 4,498,172 to Bhavsar discloses a built-in test system that employs a dual-mode feedback shift register to supply test vectors and evaluate test responses of functional and interface networks of a logic system. Test responses are supplied to a quotient bit compressor that generates a system response signature for comparison with an expected fault-free signature to producer a system pass/fail status signal.

US 4,503,536 to Panzer discloses a digital unit testing system using signature analysis. Memory 10 provides test patterns and a memory 12 provides expected test signature patterns. The response data from the unit under test are converted into a signature in signature analyzer 20. Comparator 22 compares the outputs of signature analyzer 20 and memory 12. The test patterns are applied to the unit under test in step with clock 24 and sequential counter 26.

US 4,513,373 to Sheets discloses a local area network using protocol converters 30, 32, 34 and 36 to translate to a computer 52 with an incompatible communications format.

US 4,513,418 to Bardell, Jr. et al. discloses modifying and connecting together in series the LSSD scan paths on a number of logic circuit chips to simultaneously serve as a random signal generator and data compression circuit to perform random stimuli signature generation.

US 4,514,845 to Starr discloses locating a bus fault by placing devices in a high impedance state and sensing current flow between devices.

US 4,519,078 to Komonytsky discloses LSI and discrete logic circuits, including Level Sensitive Scan Design, that incorporate internally generated pseudorandom sequences as test vectors to stimulate the logic circuits under test. Responses to the test vectors are analyzed internally or externally using signature analysis to determine if the circuit has functioned properly.

US 4,534,028 to Trischler discloses applying a first digital test pattern to the primary inputs of a complex digital circuit while a second digital test pattern is shifted into a scan path of shift registers. The digits appearing at the primary outputs are repeatedly compared with those of a first digital number indicative of the proper operation of the circuit as each digit of the second digital test pattern is shifted into the scan path shift register.

US 4,553,090 to Hatano et al. discloses a method of testing a logic circuit having a plurality of flip-flops associated with a scan path and combination circuits. The method: transforms parallel input data to serial input data, sets the serial input data in each selected flip-flop, performs a logic operation in the combination circuits on the data stored in the flip-flops, stores the resulting data in the flip-flops and outputs the output data in parallel.

US 4,575,674 to Bass, et al. discloses a diagnostic circuit for diagnosing a plurality of serially connected flip-flops in real time. See Figure 2.

US 4,577,318 to Whitacre, et al., discloses comparing A data on the 26 lines of data set A with B data on the 26 lines of data set B. The lines of A data and the lines of B data are fed to selector multiplexers 505a and 505b. The outputs of these multiplexers are fed to an EOR circuit 502 for comparison. A mask register 501 connects to the selector multiplexers in order to blank out selected input lines to multiplexers 505a,b. Mask register 501 has an input CI bus 501ci, which carries the bus control signals from bus control unit 510, which in turn connects to the D or data bus 34.

US 4,587,609 to Boudreau, et al. discloses a lockout circuit used in an asynchronous shared computer system. A first unit can lock a shareable unit to deny access to other units seeking to lock the shareable unit. Other units can access the shareable unit if they are not seeking to lock it.

US 4,594,711 to Thatte discloses a universal testing block (UTB) for on-chip testing of a VLSI subsystem such as a ROM or an ALU. The UTB can act as a test generator and a test evaluator.

US 4,597,042 to d'Angeac, et al. discloses a device for loading data in, and reading data out of a plurality of latch strings which are contained in a data processing system for testing, failure isolating and initializing. The device is operable to transmit test or initialization data to a plurality of latch strings in a system realized in accordance with the Level Sensitive Scan Design technique. In Figure 4, addressing unit Mi includes SRL latches 42, 43, and 44 providing three address bits that select one of eight strings. The three address bits are connected to string selector 48, which produces one of eight select signals 49-1 through 49-8.

US 4,597,080 to Thatte, et al. discloses a method and apparatus for testing VLSI processors using a bit-sliced bus-oriented data path including data and control monitors and BIT for the on-chip memory. The control monitor is used to decouple the testing task of the control section from that of the data path.

US 4,598,401 to Whelan discloses a signature analysis circuit. Responses to test patterns applied to the circuit under test are applied to a linear feedback signature register (LFSR). The LFSR produces a signature signal dependent upon its prior state and the responses. The outputs of the LFSR are applied as the address to a memory part having a 1 or 0 output, depending on whether the part tests true or fails. The checking occurs during the testing sequence, in contrast to conventional signature analysis testing where the analysis occurs only at the end of test.

US 4,601,034 to Sridhar discloses an apparatus for testing VLSI memory elements including a parallel signature analyzer.

US 4,602,210 to Fasang et al. discloses a plurality of scan paths in an IC fro testing. Each scan path includes plural bistable scan path flip-flops isolated from the combinational circuits.

US 4,612,499 to Andresen, et al. discloses a test input demultiplexing circuit in which a test signal is multiplexed with a data input line.

US 4,615,029 to Hu, et al. discloses a ring transmission network for interfacing control functions between master and slave devices. A test/maintenance controller 120 interfaces with a slave device 96 through a serial transmission line 106.

US 4,618,956 to Horst discloses testing the inputs of an ALU to see if logical AND is zero or the two inputs are equal whiles allowing the ALU to perform another function at the time the tests are made. Corresponds to EP 0,136,174 and JP 60-168,243.

US 4,621,363 to Blum discloses including interface registers in the Level Sensitive Scan Design chain of shift registers. During testing, test data and response data are effected through the interface resisters to the system bus.

US 4,627,018 to Trost, et al. discloses a system to accelerate the granting of prioritized memory requests to a multiport memory system. The system detects one remaining request in the memory, and clears the priority logic before the requestor would normally be activated to receive the next group of memory requests.

US 4,628,511 to Stitzlein, et al. discloses recording pre- and post-failure events to analyze signal activity on an input/output channel to determine failing equipment.

US 4,635,193 to Moyer, et al. discloses a data processor having selective breakpoint capability communicates with a peripheral device to set the breakpoints. The instruction execution control means receive an operand from the peripheral device and selectively store the operand in the instruction register in response to the execution of a breakpoint instruction.

US 4,635,261 to Anderson, et al., discloses an on chip test system for configurable gate arrays with plural gates coupled to inputs and outputs of the chip. The gates may asynchronously receive signals from the inputs and asynchronously send signals to the outputs. In Figure 3, input shift registers 23 and output shift registers 25 are connected in series to provide test signals to the outputs of the circuit 20, to connect to further circuits through bond pad 36 and to provide self test of the shift registers themselves. In Figure 4, input registers 23 are connected together to form a pseudo-random pattern generator 30 with outputs connected to the gates 21. The output registers 25 are connected in series to form a signature analysis register 40 receiving the outputs from the gates 21.

US 4,638,313 to Sherwood, et al. discloses addressing for a multipoint communication system for patient monitoring.

US 4,642,561 to Groves, et al., discloses compressing the amount of data stored in local test data RAMs for implementing a circuit test.

US 4,646,298 to Laws, et al. discloses a computer system having intelligent and non-intelligent processing circuits that communicate with one another through connection slots of a communication bus. Each intelligent processing circuit has an identity memory and can specify in the memory that it performed and passed a self-test. The intelligent processing circuits that have passed the self-test arbitrate among themselves, based on their position on the communication bus, to determine which is to become the system test master to test the rest of the system and the non-intelligent processing circuits.

US 4,646,299 to Schinabeck, et al. discloses applying static analog voltages or currents to pins of a device under test and measuring resulting currents or voltages to evaluate the responses of the device being tested.

US 4,651,088 to Sawada discloses a logical and electrical characteristics tester having a measuring circuit corresponding to each pin on the device under test.

US 4,669,061 to Bhavsar discloses a scannable flip-flop that can be used in testing combinational logic with test vectors.

US 4,672,307 to Bruer, et al. discloses testing combinatorial circuits by applying 1-transitions to the inputs. The accuracy of the outputs are checked by signature analysis or otherwise. An appropriate Gray code of 1-transistions are obtained from a ring counter and conventional counter.

US 4,674,089 to Poret, et al. discloses an in-circuit emulator (ICE). Capture logic 15 captures the contents of the program address register (PAR), the internal data bus (IDB), and various microprocessor 13 control (CONTROL) lines. The capture logic 15 provides outputs on lines 45 to trace circuits 25. Trace circuits 25 use a FIFO buffer to transfer the captured data to the output pins 31 of the chip 11. A content addressable memory 17 and a software programmable logic array 21 operate as a finite state machine to perform testing. The content addressable memory 17 determines the status of the processor and compares it with a set of four possible word recognizers with comparators 61. The content addressable memory 17 and software programmable logic array are apparently loaded from the microprocessor 13 over lines 41 through mode control 27 and lines 43.

US 4,679,192 to Vanbrabant discloses an arrangement for an orderly transmission of digital data between stations S1-Sn connected to a common communication path B. A main station distributes clock pulses on the communication path B. The clock pulses are counted in the stations S1-Sn. When the station number and the counting position agree, the relevant station is enabled to transmit data to one of the other stations.

US 4,680,539 to Tsai discloses a linear feedback shift register for inclusion in a level sensitive scan design (LSSD). A scan cell S4 includes a one bit register 23, see Figure 7, two exclusive NOR gates 19 and 20 and additional gates. Corresponds to EP 0,148,403 and JP 60-147,660.

US 4,680,733 to Duforestel, et al. discloses a device for serializing/deserializing bit configurations of variable length for loading and reading bit configurations in strings of latches.

US 4,683,569 to Rubin discloses connecting test points to shift registers that are read out bidirectionally. The data in the shift registers is shifted in each direction and compared to a reference data signal to indicate an error in a test point.

US 4,687,988 to Eichelberger, et al. discloses applying pseudo-random patterns in parallel to each of the inputs of an IC using LSSD design rules, forming an output signature and comparing the signature to a known good signature. Corresponds to US 4,745,355; and US 4,801,870.

US 4,694,293 to Sugiyama, et al. discloses a circuit used in an electronic musical instrument in which a number of musical tone generating circuits (receivers) are fed with different tone data by a single control circuit to produce different tones simultaneously.

US 4,698,588 to Hwang, et al. discloses a transparent shift register latch 170 for isolating peripheral ports during scan testing of a logic circuit. See Figure 8. The latch includes internal isolation gate 186. Corresponds to 5,032,783.

US 4,701,916 to Naven, et al. discloses an integrated circuit having plural registers. In operation, the registers act as parallel input/output registers. In a shift mode, the registers form a serial shift path and in a test mode, the registers act as a pseudo-random number generator and a signature analyzer.

US 4,701,920 to Resnick, et al. discloses built-in self test circuitry 10 for LSI circuit chips. The test circuitry includes a serial scan path (TDI-TDO) and control signal logic 42. Input register 36 applies test signals to the main logic function 14 and output register 38 receives output signals from the main logic function 14.

US 4,701,921 to Powell, et al. discloses a modularized scan path for serially tested logic. Modules 26 each have serial registers 34-40, input gate 48 and output gate 50. Address 16 and

control 12 leads connect to address decode/select 52, which selectively connects the scan data in leads 28 and the scan data out leads 30 to the modules for testing. Corresponds to US 4,710,931 and US 4,710,933.

US 4,710,931 to Bellay et al. discloses a test partionable logic circuit comprising plural functional modules 26a-n. Each functional module interfaces to the exterior of the logic circuit with a data bus 20, an address bus 16 and a control bus 12. Each module is addressable through an address decode/select circuit 52 to operationally isolate the select modules and define a test boundary. Test data is scanned into a serial chain of shift register latches that are connected in a daisy chain configuration. The defined test boundary allows each module to be separately selected and tested to provide a separate and distinct test program for an individual module. Corresponds to US 4,701,921 and US 4,710,933.

US 4,710,932 to Hiroshi discloses comparing cross correlation values from a device under test and a reference device where the values from both devices are counted with no delay and with delays made in steps to a predetermined time interval.

US 4,710,933 to Powell, et al. discloses a parallel to serial scan system for testing logic circuits. Parallel registers 72-80 receive operational and test data from a common bus 70 and are selected by decoder 104. The test data passes through combinational logic and the responses are captured in serial register latches 92-102. Corresponds to US 4,701,921, and US 4,710,931.

US 4,734,921 to Giangano, et al. discloses a fully programmable linear feedback shift register. A polynomial equation is first fed into the linear feedback shift register for setting the respective flip-flops into predetermined logic states, which are used to encode messages to be shifted by the programmable linear feedback shift register. Corresponds to WO 88/04097, EP 0,290,589, and JP 1-501,979.

US 4,740,970 to Burrows, et al. discloses a specific use of gates in a Built-In Logic Block Observation. Corresponds to EP 0,190,494 and JP 61-217,779.

US 4,743,841 to Takeuchi discloses a circuit selectively connecting an operative circuit or a test circuit to the bond pads of an integrated circuit.

US 4,752,929 to Kantz, et al. discloses testing a semiconductor memory part by subdividing the memory array into cell fields and comparing data bits in corresponding storage cells of each field.

US 4,759,019 to Bently, et al. discloses a programmable fault injection tool for testing a digital processing system. The tool injects faults for a user specified time duration and only after a user specified time delay.

US 4,763,066 to Yeung, et al. discloses comparing four digital test signals to known good reference signals. The four test signals are the result of analog horizontal and vertical signals directed to an integrator/A-D.

US 4,764,926 to Knight et al. discloses an integrated circuit having a built-in self test facility. The combinatorial logic is divided into sub-circuits A-F that are fed and observed by series connected registers flip-flops 1-8. See Figure 3. Multiplexers M4-M6 select the serial input to each register to include the output of down stream registers. See Figure 7. Corresponds to EP 0,195,164 and JP 61-155,878.

US 4,777,616 to Moore, et al. discloses a logic analyzer instrument that acquires digital samples from plural logic signals in a main frame computer and displays the edges of the signals enlarged and with precision.

US 4,783,785 to Hanta discloses diagnosis of logical circuits. Input latches 6 capture test data and apply it to combinatorial circuits 5. An output latch 7 captures the response data. Circuit 19 compares the response data to known good data. Corresponds to DE 3,700,251 A1 and JP 62-159,244.

US 4,788,683 to Hester, et al. discloses a converter between a system processor and a support processor for controlling testing of the system processor. A parallel-to-serial and serial-to-parallel converter conveys LSSD test signals between the two processors.

In Fig. 3A, debug logic includes an instruction address comparator 11 and an instruction op-code comparator 12. Select logic 13 determines which comparator output is selected. An instruction compare address register 14 and an op-code compare address register 16 are accessible by the LSSD scan strings on line 30a, and contain the desired instruction and op-code compare values, respectively. In addition to the selection between stop on instruction address or op-code made by the selection logic 13, stop enable logic 17 contains a single latch bit to enable the stop-on-address function.

One output is provided for the compare output 18 and a separate output is provided for the stop-on-address function 19. The compare output from 18 can be used as a sync pulse to an external logic analyzer. The stop output from 19 is used in conjunction with the external clock generator to disable the clocks when the stop address is detected. A third output 21 is provided which toggles each time an instruction is executed. This "Instruction Complete" output is required to implement an instruction single step function, since instructions may take more than one cycle to execute. (21 OCT 03)

US 4,791,358 to Sauerwald, et al. discloses a method of testing an interconnection between two integrated circuits which are mounted on a carrier and which are interconnected by data connections, for example a printed wiring board. The integrated circuits are also connected to an

I^2C serial bus via which test patterns and result patterns can be communicated. Corresponds to US 4,879,717.

US 4,799,004 to Mori discloses a transfer circuit for operational test of LSI systems. Serial scan registers connected in series shift test data to the inputs of functional blocks 11 and 12 and serial scan registers capture the response data from the functional blocks and shift the response data out.

US 4,799,052 to Near, et al. discloses a method of determining access on an electronic serial bus by implicit token passing. Each device on the serial bus includes a bus access timer that carries a unique value for that device. Each bus access timer begins counting at an end of transmission signal on the bus and stops either when the count equals a unique count for that device or at a start of transmission signal on the bus.

US 4,800,418 to Natsui discloses an integrated circuit having a reference element selectively operated by an over-voltage applied to a bonding pad.

US 4,802,163 to Hirabayshi discloses a test facilitating circuit. Serially connected latches F1-F6 are interposed between modules M1-M3.

US 4,808,844 to Ozaki, et al. discloses a bonding pad selection switch circuit connecting a bond pad to an internal circuit in response to a control signal applied to another bond pad.

US 4,811,299 to Miyazawa, et al. discloses a DRAM part that enters a test mode upon the combination of a column address strobe signal, a row address strobe signal and a write enable signal, which normally do not occur together. Corresponds to US 4,992,985; US 5,117,393, and JP 62-250,593.

US 4,812,678 to Abe discloses a through passage circuit selectively short-circuiting an input circuit to an output circuit. Corresponds to DE-A-3,709,032 and JP 62-220,879.

US 4,817,093 to Jacobs, et al. discloses testing a multi-chip packaged structure by isolating the one chip under test, applying test signals to that chip, creating a signature of the response signals from that chip and comparing the signature to that of a known good chip.

US 4,819,234 to Huber discloses a debugger, which performs several different functions including identifying and inserting breakpoints, that is part of the operating system of a processor with virtual memory.

US 4,821,269 to Jackson, et al. discloses a diagnostic system for a digital signal processor that monitors various internal test points within several modules. Any test point can be connected to a diagnostic bus for display from an output module.

US 4,825,439 to Sakashita, et al. discloses having an operating mode in which operational signals are output in parallel and a test mode in which serial input test signals can be output in parallel and the operational signals can be output as serial output response signals.

US 4,833,395 to Sasaki, et al. discloses signal generators 11 and 12, input buffer 13 and output buffer 16 for testing a logic circuit 14.

US 4,833,676 to Koo discloses a method and apparatus for testing for stuck open faults in integrated circuits 10 having a plurality of combinational logic devices 18, 20. A chain of shift registers 22 each include latches L1 and L2 for holding respectively the detection test pattern and the initialization test pattern. See the scan cell of Figure 2.

US 4,855,954 to Turner, et al. discloses an in-system programmable device, using non-volatile programmable memory cells, that may be configured or re-configured while installed in a user's device. The normal device inputs and outputs are isolated during programming.

US 4,857,835 to Whetsel discloses a global event qualification system. The system provides the timing and control required to activate an IC's test logic during normal functional operation. The input and outputs of an IC are bordered by unique comparator cells or Event Qualifier Cells (EQCELL). The EQCELLs compare the data entering or leaving the IC to test data vectors loaded during a scan operation. The EQCELL generates a control signal when the comparison is true. Corresponds to EP 0,315,475.

A local controller 24 is used to control built-in test logic in logic core 22. The control lines necessary for this are indicated by bus 8. The local product terms 9 and 31 are ANDed by AND gate 30. This generates a global product term on bus 5. The global product term on bus 5 is fed back into the local controller 24. This allows the local controller to react to the occurrence of a global event. The local controller 24 will start the test of logic core 22 when bus 5 changes state.

US 4,860,288 to Teske, et al. discloses a test system including a ring oscillator distributed around the periphery of the VLSI chip and an I/O cell connected to each signal pin, from which are built the serially connected input registers and output registers. This provides a more accurate measurement of clock skew by providing a clock monitor pin directly connected to the clock bus internal to the VLSI chip. Corresponds to US 4,912,709.

US 4,860,290 to Daniels, et al. discloses a logic circuit having individually testable logic modules. Each of the modules may be selected for testing by means of a scan path in the module made up of serial register latches (SRLs) 34. Each module has a test port 28a.

US 4,862,071 to Sato, et al. discloses high speed circuit testing apparatus having plural test conditions. See Figure 10. Level comparison sections 300 receive an output from circuit under test and reference voltages H and L. The outputs of the level comparison sections 300 become the inputs to logical comparison sections 400. Each logical comparison section 400 includes signal detectors 402 and 403 respectively detecting the presence of the response signal using the strobe pulses STRB 1 and STRB 2.

US 4,862,072 to Harris, et al. discloses a set of four pins of an LSI chip providing access by a serial data line to macrocells or other partitioned logic of the LSI for individual test. The macrocells are connected to the remainder of the logic by a pair of multiplexer/test register combinations, one at the input and one at the output of the macrocell.

US 4,864,570 to Savaglio, et al. discloses a processing pulse control circuit for use in treating indeterminate signature increments in an apparatus producing RPT signature analysis of digital circuits. A memory stores clock count values where indeterminate signature increments will be encountered.

US 4,864,579 to Kishida, et al. discloses scan registers provided between circuit blocks.

US 4,866,508 to Eichelberger, et al. discloses, see Figure 4, loading test data into serial latches SR2A and SR2B, passing the test data through the circuits under test, such as latch 21c, counter 21b and "general" logic 21a, and capturing the resulting test data in serial scan latches SR1A and SR1B.

US 4,870,345 to Tomioka, et al. discloses gate circuits 70-74 connected to the outputs of scan registers 8-13 and 16 to control the input to the next circuit block, such as circuit block 36.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path can be compressed or expanded to pass only through the desired logic element(s) to be tested. Corresponds to JP 63-308,583.

US 4,875,003 to Burke discloses using a LSSD boundary scan chain to test input and output cells of a circuit.

US 4,878,168 to Johnson, et al. discloses applying serial test information through a serial bus to a storage control unit that interfaces a processor and a storage unit. The control unit changes the serial data from the serial bus to parallel data normally provided by the processor. The test information thus becomes indistinguishable from parallel data applied directly from the processor along a parallel bus.

US 4,887,262 to van Veldhuizen discloses a single-channel bus system for multi-master use with bit cell synchronization, and master station comprising a bit cell synchronization element suitable for this purpose.

US 4,887,267 to Kanuma discloses a logic circuit having a FIFO memory circuit to store values from a test node. The FIFO memory then is unloaded to trace the outputs of such as the states of an internal bus.

US 4,893,072 to Matsumoto, et al., discloses testing an IC device 21 that includes a logic circuit section L and a memory circuit section M. Logic circuit section L includes flip-flops 30, 31, 32, and 33 that provide time delays between input and output signals through the IC 21. An IC-device testing apparatus 23 includes flip-flop circuits F11, F21, F22, ..., Fnn, that provide for matching the time delays through the logic circuit section L of actual test signals applied to the IC 21 and expected signals EX. The IC tester applies a test signal to an IC under test and an expected response signal to the input of a shift register. The shift register is clocked to produce the

expected response signal at its output at the same time the IC should produce its response to the test signal. The tester then compares the expected response signal to the actual response signal.

US 4,894,830 to Kawai discloses an LSI chip with scanning circuitry for generating reversals along activated logical paths. A pulse is scanned along first flip-flop circuits to propagate test signals through the activated logical paths. A second string of flip-flops connect to the outputs of the logical circuits and are configured into a linear feedback shift register to determine the dynamic performance of the logic circuit.

US 4,896,262 to Wayama, et al. discloses a memory system having a semiconductor memory providing faster access than a magnetic disk storage system.

US 4,897,842 to Herz, et al. discloses a signature generator connected to plural circuit nodes to be tested.

US 4,899,273 to Omoda, et al. discloses a clock-synchronized simulation method of simulating the logic operations of combination circuits between flip-flops, while operating the flip-flops at a constant time, by using clock signals as conditions for setting and resetting the flip-flops.

US 4,903,266 to Hack discloses a system and method for on-chip self test of memory circuits. The testing includes a random pattern generator addressing all memory locations and using a linear feedback shift register to generate a signature of the test results. A level sensitive scan design serial bus can test all logic and the combination can provide a final test signature.

US 4,907,230 to Heller, et al. discloses a device comparing the digital or analog outputs of circuit boards or other units under test with known good models. A clip connects each point of the circuit under test to a pin of the test instrumentation.

US 4,910,735 to Yamashita discloses an integrated circuit having plural logic blocks. Each logic block has an operational circuit, a pattern generator, and a switching circuit for selecting either an operational input signal or the pattern signal as the input to the operational circuit. Corresponds to EP 0,273,821 and JP 63-153,483.

US 4,912,633 to Schweizer, et al. discloses an hierarchical multiple bus computer system including a master bus and slave buses, which master and slave buses are substantially identical. Communication between the master bus and a slave bus is effected through a combination of an interface controller 12, a shared dual port RAM 14 and a shared RAM controller 13.

US 4,918,379 to Jongpier discloses providing an integrated circuit with macro circuits that can be individually tested. A test bus extends along the integrated circuit and connects with a test interface circuit in each macro circuit. The test interface circuits are connected in series.

US 4,924,468 to Horak, et al. discloses a logic analyzer measuring signals that are delivered by a number of targets, such as microprocessors, that are not correlated in time.

US 4,926,425 to Hedtke, et al. discloses a system for testing successive component groups separated by accessible nodes. The process observes data at the nodes and supplies test data to the nodes.

US 4,929,889 to Seiler, et al. discloses a test/load bus internal to an integrated circuit to supply test data to test nodes internal of the chip and unload response data from the test nodes.

US 4,930,216 to Nelson discloses a process for preparing integrated circuit dies, while still in wafer form, for surface mounting direct to a substrate without requiring packaging of the dies and maintaining corrosion resistance.

US 4,931,722 to Stoica discloses serial scan paths of registers for serially scanning test data into and out of the registers, applying the serial test data in parallel to combinational logic between the paths and receiving parallel test result data from the combinational logic.

US 4,931,723 to Jeffrey, et al. discloses a test device having plural tester channels. Each channel has a channel control circuit means coupled to a pin of a unit under test for controlling the state of operation of the pin.

US 4,935,868 to DuLac discloses an integrated circuit for interfacing a standard IEEE 796 bus to a VSB-type buffer bus. the circuit includes a DMA channel for high speed access of the IEEE 796 to the buffer bus and a slave bus channel for high speed access of the buffer bus to the IEEE 796 bus. A third bus interface connects to a local processor to assist in arbitration and control during some types of data transfers.

US 4,937,826 to Gheewala, et al. discloses pre-charging sense lines to known signal levels immediately prior to using the sense lines to sense the signal level at a test point. This eliminates the need for sequential patterns to detect "stuck-open" faults.

US 4,943,966 to Guinta, et al. discloses a serial diagnostic bus (SDB) connecting to a memory control unit. Over the SDB, the system console 30 can read from and write to registers in memory boards 12 and 14.

US 4,945,536 to Hancu discloses connecting input and output signals to a boundary scan register, using three types of boundary scan cells 230, 240 and 250.

US 4,947,106 to Chism discloses a test module testing an analog to digital converter by deterministically checking higher order bits and non-deterministically checking lower order bits.

US 4,947,357 to Stewart, et al. discloses a circuit board carrying plural integrated circuits, each with an internal scan chain. The scan input of each integrated circuit is connected to a system scan controller 26. The scan outputs of the integrated circuits are connected to multiplexer 30 for selective testing of individual integrated circuits.

US 4,956,602 to Parrish discloses wafer scale testing of redundant integrated circuit dies. In Figure 2, wafer test pads 14 are selectively connected by input/output buffer circuit 16 to dies 12 to carry test signals to the dies and carry response signals back to the test pads. Corresponds to US 5,053,700.

US 4,961,053 to Krug discloses arranging test circuits on a wafer, the wafer also carrying the integrated circuits to be tested. Power is applied to the wafer and testing occurs automatically.

US 4,969,121 to Chan, et al. discloses an integrated circuit programmable logic array circuit with improved microprocessor connectability.

US 4,974,192 to Face, et al. discloses a communications processor 46 for a personal computer. Corresponds to WO-A-89 01,202.

US 4,974,226 to Fujimori, et al. discloses comparing data stored in a data register 13a with a 1 bit signal stored in a scan latch 1c to determin coincidence or non-coincidence therebetween.

US 4,989,209 to Littlebury et al. discloses an interface apparatus for coupling a multi-channel tester to high pin count integrated circuits. Test stimulus data is applied in parallel to circuits 21 through shift registers 16 and 18. Test response data is assembled in register 17 and returned to tester 11.

US 5,001,713 to Whetsel discloses an event qualification testing architecture. A boundary test architecture uses input and output test registers 12, 22 having functions controlled by an event qualifying module (EQM) 30. In response to the EQM receiving a matching condition signal from the register 22, the EQM may control the test registers 12, 22 to perform a variety of tests on the incoming and outgoing data. The internal functional logic 20 may continue to operate at speed during the testing to determine faults not otherwise discoverable. Corresponds to US 5,103,450; EP 0,382,360, and JP 3 020,683.

US 5,008,618 to Van Der Star discloses testing circuits having mutually asynchronous clock signals. The test device provides separate scan chains for stimulus and response patterns for the element sets controlled by each clock signal. The test device performs a separate test sub-cycle for each scan chain.

US 5,008,885 to Huang, et al. discloses inserting errors into parts at controlled times through programmable masks.

US 5,012,185 to Ohfuji discloses an integrated circuit having a function for checking whether input/output terminals of the integrated circuit are properly connected to wirings on a printed circuit board.

US 5,014,186 to Chisholm discloses a data processing system having a bus system coupling I/O units to a storage unit. The I/O units are supplied a line size signal representing the line size of the storage unit. The I/O units respond to this line size signal to adjust the data transfer size or packet of the I/O unit to match the storage unit line size.

US 5,023,872 to Annamalai discloses simple error detection logic with an error counter and a timer detects errors in a dual token ring network.

US 5,042,005 to Miller, et al. discloses a timer circuit with match recognition features.

US 5,048,021 to Jarwala, et al. discloses generating a control signal to control the test activity of a boundary scan system. A macro controller shifts bits out of a register indicating the macro's identity and shifts the same bits back into the register to maintain the identify indicated by the bits.

US 5,051,996 to Bergeson, et al. discloses a built-in test by signature system that provides fault detection by the bits in the signature detection logic.

US 5,053,949 to Allison, et al. discloses a debug peripheral that uses externally provided instructions to control a core processing unit.

US 5,054,024 to Whetsel discloses a system scan path architecture, provided by a device select module (DSM) 18. The DSM selects secondary scan paths (PATH1-m) on each circuit for coupling with a primary scan path on a test bus 14. Remote bus masters 124 may be used in conjunction with the DSMs to provide serial-scan testing independent of the primary bus master 12. Corresponds to 5,056,093.

US 5,056,094 to Whetsel discloses a delay fault testing system. A special test instruction to a boundary test cell invokes a toggle mode that allows the output boundary of an IC to output a transition between logic states on the edges of a clock signal. The same test instruction configures a boundary test cell of a receiving IC to sample input data on the subsequent edge of the clock signal. The sampled data can be inspected to determine whether the output signal propagated to the receiving IC in the prescribed time.

US 5,070,296 to Priebe discloses a test system for determining the integrity of interconnections between integrated circuits. The values on the inputs of the integrated circuits are set, in the absence of input signals reaching them, by switchable resistances in the corresponding test circuit portions. The switchable resistances can couple a predetermined signal value to a corresponding input but can also be overridden by signals supplied to that input across the corresponding interconnection.

US 5,070,297 to Kwon, et al. discloses a full wafer testing device with, see Figure 2, probe tips 16.

US 5,077,740 to Kanuma discloses testing individual macrocells of a logic circuit by shifting test data into register 12, shutting off an input path for normal operation signals to the macrocell, and applying the test data in register 12 to the macrocell. An output register 14 receives the output of the macrocell under test and the contents of register 14 is shifted out, while shutting off an output path of normal operating signals from the macrocell.

US 5,084,814 to Vaglica, et al. discloses a CPU having access to on-chip and off-chip peripherals and memory in both a normal and alternate mode of operation by means of a parallel bus, which it operates as a bus master. In an alternate mode, the CPU receives instructions on a serial bus on which the CPU is a slave device.

US 5,084,874 to Whetsel discloses a testing buffer register 12. See Figure 2. The test cell can also include compare and other logic. See Figures 6 and following. Corresponds to US 5,495,487; US 5,602,855; US 5,631,911; US 6,081,916; US 6,304,987; and US 6,611,934.

US 5,090,015 to Dabbish, et al. discloses a self checking electronically erasable programmable array logic. The device verifies the storage integrity of each cell within the array

during programming, after completing programming, and prior to executing the algorithm stored in the array.

US 5,090,035 to Murase discloses a linear feedback shift register. This arrangement is used to control the generation of polynomials through the feedback register.

US 5,107,148 to Millman discloses a block isolation buffer including a circuit for providing predetermined voltage levels at the inputs of the circuit blocks which are not being tested, thereby assuring that an undesired input does not appear at the inputs of the non-tested circuit blocks.

US 5,107,489 to Brown, et al. discloses a dynamic switch for use in establishing dynamic connections in a link by use of frames. Each frame has an identification of the source of the frame, an identification of the destination of the frame and link controls to maintain, initiate or terminate a connection between the source and destination. The state of the dynamic witch port is changed dependent upon its present state, the dynamic connection requested, and the direction and type of frames passing through it.

US 5,109,190 to Sahashita, et al., discloses semiconductor integrated circuit including a circuit block, a plurality of boundary scan registers, a system data terminal, a test signal terminal and a control circuit. The control circuit generates control signals for controlling the boundary scan registers. The boundary scan registers are connected in cascade to each other and each is connected to the circuit block. Each boundary scan register, Figure 6A, includes a selector circuit 12 and latch circuits. Latch circuit 13 shifts in data of an adjacent preceding boundary scan register and also captures data from the selector circuit. The selector circuit selects system data

or test data. The latch circuit 14 shifts the captured data to an adjacent succeeding boundary scan register. The latch circuit 15 applies the selected data to the circuit block.

US 5,109,383 to Chujo discloses scan path latch circuits. The latch circuits include three switches and two flip-flops

US 5,115,191 to Yoshimori discloses a boundary scan testing integrated circuit adapted to both a functional test of an entire IC and a parametric test for input and output buffers.

US 5,115,435 to Langford, II et al. discloses using the power and capability of existing address and data buses to transfer boundary scan test data into and out of the ASIC or VLSI circuit.

US 5,126,286 to Chance discloses a method of making edge connected integrated circuit dies.

US 5,128,664 to Bishop discloses a search technique for identifying slave devices connected to a serial bus. When a master controller senses a condition that requires a condition that requires an assessment of devices on the bus, it examines the addresses of previously connected devices at more frequent time intervals than it does for addresses that were not previously associated with connected devices.

US 5,130,988 to Wilcox, et al., discloses IEEE 1149.1 boundary scan chain configured to permit fault insertion testing of diagnostic and maintenance software. Each scan cell includes storage devices for two bits of information, one bit is faulty data and the other serves to control application of the faulty bit.

US 5,132,635 to Kennedy discloses JTAG serial testing of removable circuit boards on a backplane bus. In Figure 2, each pc-board includes a slot occupied detector circuit 195. In response to detecting over line 180 the presence of a pc-board in the next adjacent slot, the circuit passes the serial test data to the next pc-board or to the return serial test data line 160.

US 5,133,062 to Joshi, et al., discloses a RAM buffer controller for providing simulated first-in first-out (FIFO) buffers in a random access memory.

US 5,134,314 to Wehrmacher discloses a method and circuitry to prevent tester induced failures and reliability problems that occur when a tester creates bus contention by overdriving output pins of an integrated circuit. For each input/output (I/O) pad which is used for the output of data, a first signal on an output data line is compared with a second signal which is currently on the I/O pad. When the output is enabled and the comparison indicates the first signal is not equal to the second signal, the I/O pad is isolated from the output data line. The I/O pad is isolated, and thus in shutdown mode, until the I/O pad is no longer being driven to a signal value which is different than the signal value of the first signal on the output data line. Further, each I/O pad may be electrically isolated from its output data line whenever a comparison for any I/O pad indicates that the signal for the I/O pad is not equal to the signal on its output data line. In one embodiment, once all of the I/O pads are in shutdown mode, they are held in shutdown mode until a reset signal is received.

US 5,150,044 to Hashizume, et al. discloses a semiconductor integrated circuit comprising scan paths having individually controllable bypasses.

US 5,150,047 to Saito, et al., discloses a member for assembly of ICs having a large number of connection terminals and a self-test circuit. The member comprises conductive leads formed on one surface to be connected to connection terminals of the IC element, and a limited

number of test pads. The number is not smaller than the number of the conductive leads for connection to the connection terminals associated with the test circuit, but irrespective of and less than the number of all the conductive leads of the IC element. The conductive leads are selectively connected to the test pads so that electrical connections between the conductive leads and the connection terminals and/or the functions of the IC elements can be tested through the test pads. The test pads are formed with a size of each pad and a space between any two pads large enough to assure the reliability of the test without increasing the space of a margin area of the member on which the test pads are provided.

US 5,155,432 to Mahoney discloses a system for scan testing of logic circuit networks. Switching means are selectively varied to provide different test circuit configurations for different modes of operation.

US 5,159,465 to Maemura, et al. discloses a facsimile machine having a transmission speed selective downshift function. A common buffer memory provides for temporarily storing coded image information either in an Error Correction Mode or a normal transmission mode.

US 5,161,160 to Yaguchi, et al. discloses scan paths SP100-SP107 connected to different bus lines IB0-IB7, respectively.

US 5,165,022 to Erhard, et al. discloses a computer system having a universal channel and control unit to interface to a plurality of different I/O adapters such as Token Ring or Ethernet.

US 5,167,020 to Kahn, et al. discloses a serial data transmitter with dual buffers operating separately and having scan and self test modes.

US 5,170,398 to Fujieda, et al., discloses a test pattern generating device for a memory having a logical operation function. The device uses a pattern generator and a tester CPU to generate address and data that are compared to the output of a device under test.

US 5,172,377 to Robinson, et al. discloses a method for testing mixed scan and non-scan circuitry using a boundary scan facility. The testing isolates the non-scan components and either drives or senses voltages at physically accessible test sites.

US 5,173,906 to Dreibelbis, et al., discloses a built-in self test for integrated circuits. A deterministic data pattern generator is provided on the VLSI chip, and operates to test a chip module and provide a fail/no-fail result, along with data identifying where the fail occurred.

US 5,175,447 to Kawasaki, et al., discloses a multifunctional scan flip-flop having a normal function and a scan function. A first latch, used for a normal function, latches input data applied to a data input terminal, the latch operation being carried out synchronous with a clock applied to a clock input terminal. A second latch, used for a scan function, holds scan data applied to a scan data input terminal. A delay circuit delays one of the input data and the clock relative to the other, the delay operation being carried out in accordance with the H/L level of the scan data held by the second latch.

US 5,187,795 to Balmforth, et al. discloses a pipelined signal processor having plural bi-directional configurable parallel ports that are configurable as individual ports or as coupled pairs of ports.

US 5,191,653 to Banks, et al. discloses an I/O adapter for system and I/O buses having different protocols and speeds.

US 5,202,625 to Farwell discloses a bidirectional boundary scan circuit cell for use in boundary scan testing of device interconnections. The cell includes a scan flip-flop. A first multiplexer is responsive to the scan flip-flop and to a device output, if the associated pin is for an output function, for controllably providing as its output a replica of the scan register output or the device output. A three-state buffer is responsive to the output of the first multiplexer and has its output connected to the associated device I/O pin. An input buffer has an input connected to the associated device input/output pin and whose output comprises an input to the device, if the associated I/O pin provides an input function. A second multiplexer is responsive to the input buffer and a serial scan input for controllably providing as the input to the scan flip-flop a replica of the output of the input buffer or a replica of the serial scan input. For scan test purposes, the scan cell is configurable as a transmit cell for driving the associated I/O pin or as a receiver for storing the signal at the associated I/O pin.

US 5,206,545 to Huang discloses a digital output buffer including a driver capable of driving an output signal up to a maximum drive level and a driver controller responsive to contention at the driver's output and operative to reduce the drive of the driver below the maximum drive level when contention is detected. The method for reducing contention at the output of a digital buffer includes the steps of sensing the desired output of a digital buffer, sensing the actual state at an output node of the digital buffer and reducing the output drive of the digital buffer when the desired output is in contention with the actual state at the output node.

US 5,210,759 to DeWitt et al. discloses scan testing using latches for selectively observing test data. Plural Master-Slave latches observe the outputs of plural data path drivers activated during a scan test operation. The series connected Master-Slave latches then are scanned to provide the test operation data. Figure 4 provides a schematic of the Master-Slave latch.

US 5,214,760 to Hammond, et al. discloses an adaptable multi-port data buffer.

US 5,214,774 to Welsh, et al. discloses segmented memory transfer and message priority on a synchronous/asynchronous data bus.

US 5,218,702 to Kirtland discloses a system for selecting request for a resource before decoding of requested resource address and validating selection thereof.

US 5,241,265 to McDonnell, et al. discloses a logic function circuit with an array of data stores and their circuit testing with a chain of M x N flop-flops. The M x N array of logic circuits uses one multiplexer for mode selection and one logic circuit for each column of flip-flops.

US 5,241,266 to Ahmad, et al. discloses fabricating integrated circuits on a wafer with an additional layer of metal interconnects. The interconnects provide power to all the integrated circuits during testing and burn-in while the integrated circuits are still on the wafer.

US 5,252,917 to Kadowaki discloses a scanning circuit for test. The circuit includes a first selecting circuit for selecting one of a normal data signal and a scanning data signal by a first control signal and for transmitting the selected data signal. A second selecting circuit selects one of a normal clock signal and a scanning clock signal by a second control signal and for transmitting a first clock signal based on the selected clock signal. A data transferring clock signal generating circuit generates a second clock signal based on a clock signal for transferring data. A latch section is connected to the first selecting circuit, the second selecting circuit and the clock signal generating device for receiving the selected data signal, the first clock signal and the second clock signal and for outputting a signal corresponding to the selected data signal defined by a logical product of the first clock signal and the second clock signal.

US 5,254,942 to D'Souza et al. discloses a single integrated circuit providing an IEEE 1149.1 test architecture. The single chip can be connected to the inputs and outputs of a device under test, on a circuit board or on a wafer, to perform boundary scan testing of the device.

US 5,258,985 to Spence et al. discloses a combinational data generator and analyzer for built-in self test (BIST). The BIST generates a series of test vectors with a linear feedback shift register and applies the vectors to the circuit under test. The test response data is routed back and accumulated in a predetermined manner in the linear feedback shift register to provide a test signature. The accumulating test signature may be used as a subsequent test vector in the circuit under test.

US 5,260,949 to Hashizumw, et al., discloses that test data applied serially from a data input terminal is bypassed by a selecting circuit in modules that are not the object of testing and is applied to a scan path in modules that are the object of testing. Test data is applied to the control point of the functional module from the scan path, and test result data is provided from the observation point of the functional module to the scan path. The scan path shifts the test result data serially from a data output terminal. Selecting means operates in response to the selecting data held in the corresponding selecting data holding/propagating circuits. These selecting data holding/propagating circuits shift and hold selecting data applied serially from a data input terminal.

US 5,276,807 to Kodama, et al. discloses bus interface synchronization circuitry for reducing time between successive data transmission in a system using an asynchronous handshake.

US 5,278,494 to Obigane discloses a wafer probe testing machine including a loading/unloading section, a test section, an elevator, and a wafer transfer system.

US 5,279,975 to Devereaux, et al. discloses a method of testing individual dies on a semiconductor wafer prior to singulation. The method provides test circuits on each die and forms conductive paths over the wafer to provide power to each die during burn-in testing. Corresponds to US 5,461,328.

US 5,286,656 to Keown, et al. discloses AC testing of integrated circuit dies on a wafer using DC testing of known test structures on each die.

US 5,291,025 to Smith discloses inspection of wafer boats in a semiconductor wafer fabrication facility to determine automatically whether certain mechanical dimensions of a wafer boat are within specification.

US 5,297,277 to Dein, et al. discloses a monitoring device for tracing OEMI channel data and tags using a trace memory and time stamps.

US 5,303,148 to Mattson discloses a voice recognition system for doctors in surgery. The machine compares received audio to stored known words and displays the words on a screen.

US 5,313,158 to Joosten, et al.discloses a test system on a substrate. The test system uses connection terminals for selecting the test structures as well as for the supply voltages and the output of the signals to be measured. The test structures can be resistors.

US 5,315,241 to Ewers discloses a substrate to which integrated circuit dies are attached and wire bonded. Testing then occurs to all of the dies on the substrate. After testing, the substrate is divided for each die and the die and its substrate portion are used individually on printed circuit boards.

US 5,317,205 to Sato discloses a semiconductor integrated circuit having a sequential circuit including a plurality of flip-flops that latch and keep data supplied to an input terminal at a prescribed timing and perform prescribed sequential treatments of the input data. A combinational circuit is implemented at the input and/or output terminals of the sequential circuit and performs a prescribed combinational treatment or treatments of the input and/or output data to and/or from the sequential circuit. The semiconductor integrated circuit also includes a data-through circuit operated by an external control signal configured to transfer the data supplied to the input terminal direct to an output terminal of a prescribed flip-flop of the plurality of flip-flops constituting the sequential circuit.

US 5,319,754 to Meinecke, et al. discloses a data transfer system between a computer and a host adapter using multiple arrays.

US 5,321,322 to Verheyen, et al. discloses a programmable interconnect architecture without active devices.

US 5,329,471 to Swoboda et al. discloses an emulation system using state machines for a microprocessor. The system provides emulation, simulation and testability without physical probing or special test fixtures. The system provides a serial scan testability interface having first and second scan paths. The first scan path is provided for applying digital information to the functional circuit for use in emulation of the functional circuit. The second scan path connects to state machine circuits that have a sequence of states responsive to the emulation command codes. The disclosed system also incorporates a JTAG interface and has different clock signal domains. Corresponds to US 4,860,290 and US 6,522,985.

US 5,334,857 to Mennitt, et al. discloses a package substrate having solder balls on one side for electrical connection of operating circuits and carrying bond pads on the other side of the substrate for manufacture's testing of the carried integrated circuit.

US 5,343,478 to James, et al. discloses a standard JTAG test bus arrangement with an additional set of configuration registers 116. The configuration registers may include memory circuits 138, Figure 5. The configuration circuits 116 may be written to and read from to configure the operation of the computer system as well as to monitor or log errors within the computer system. The memory circuits 138 extend the amount of information that can be contained in these configuration registers 116.

US 5,353,308 to Whetsel discloses an event qualified test architecture. Event qualification cells 24 have an internal memory for detecting qualification events and output a signal indicating a match. The event qualification module controls the test registers 14,16 and test memory 28. Corresponds to US 5,623,500.

US 5,355,369 to Greenberger, et al. discloses the use of the JTAG port for boundary scan testing of integrated circuits, thereby allowing for the testing of IC's after they have been mounted into a circuit board. The present circuitry transfers the test program to a special test data register, which downloads the program to the logic circuitry under test, and uploads the results. This allows the core logic to perform the test at its normal operating speed, while still retaining compatibility with the JTAG standard for other tests.

US 5,366,906 to Wojnarowski, et al. discloses a wafer level testing package includes a dielectric layer having plural vias thereon overlying a wafer containing plural chips with pads. The vias are aligned with at least some of the pads and conductors on the layer provide connections

between the pads. The pads, vias and conductors are arranged to route boundary scan signals, and power to the chips and the boundary of the wafer.

US 5,371,390 to Mohsen discloses an interconnect substrate with circuits for field-programmability and testing of multichip modules and hybrid circuits.

US 5,377,198 to Simpson, et al., discloses a method for detecting JTAG errors in which components in a boundary scan path of a JTAG serial test bus connect a single bit bypass register into the scan path rather than the expected register when errors are detected. JTAG instruction signals are shifted into the scan path to determine whether an instruction error was received by a component. Data scanned into the component is prefixed by a header which is monitored by the JTAG control circuitry to detect any instruction errors. The combined data and header are padded by bits preceding the header to be equal to a multiple of a data register contained within the JTAG control circuitry. The least significant bit positions of the header and the padding bits are shifted out of the data register prior to the time that the header or first byte of the header should have been in the data register of the JTAG control circuitry such that the least significant bit of the data register is a 1, if no single error occurred, and is a 0 if a single error occurred.

US 5,388,216 to Oh discloses a circuit for controlling generation of an acknowledge signal and a busy signal in a Centronics compatible parallel interface.

US 5,389,556 to Rostoker, et al. discloses testing and exercising individual unsingulated dies on a wafer. External test signals are applied to bond pads on the wafer separate from the bond pads of each die. An electronic selection mechanism connects the external test signals to the dies or selected ones of the dies. Corresponds to US 5,442,282 and US 5,648,661.

US 5,389,873 to Ishii, et al. discloses a pressure contact chip and wafer testing device for burn-in.

US 5,390,131 to Rohrbaugh, et al. discloses displaying wafer test results in real time.

US 5,391,984 to Worley discloses a tester of integrated circuits. The tester selects individual test fixtures, carrying the integrated circuits, for testing. The other fixtures have stress voltages applied to them.

US 5,396,170 to D'Souza, et al. Divisional of US 5,254,942.

US 5,399,505 to Dasse, et al. discloses a semiconductor wafer having integrated circuit dice, wafer conductors, and wafer contact pads formed on the wafer. The conductors carry electrical signals to and from the dice for burn-in and functional testing.

US 5,420,874 to Kromer discloses facilitating testing of electrical circuitry that includes a circuit receiving a signal asynchronous with respect to a circuit clock. The exact clock pulse on which the asynchronous signal is asserted may be difficult or impossible to predict even when the circuitry inputs are known. However, a range of pulses can be determined during which the asynchronous signal is asserted. The sampling of the asynchronous signal is blocked until the end of the range of pulses. If it is known that at the end of the range of pulses the asynchronous signal should still be asserted provided that the circuitry functions properly, the asynchronous signal is sampled at the end of the range of pulses. Alternatively, if the asynchronous signal can be de-asserted by the end of the range of pulses, the assertion of the asynchronous signal is detected and latched by the asynchronous signal pulse detector, and at the end of the range of pulses the circuit samples the value latched by the pulse detector. In both alternatives, the end of the range

of pulses facilitates an un-ambiguous clock pulse at which the asynchronous signal should be sampled.

US 5,424,651 to Green, et al. discloses a fixture and a wafer for burn-in testing of multiple semiconductor wafers. Each wafer carries an array of integrated circuits and each integrated circuit includes its own test circuit. Each wafer also has power busses carrying power to each integrated circuit on the wafer.

US 5,426,650 to Ganapathy, et al., discloses a test circuit including a drive 1 or drive 0 scan element which utilizes fewer transistors than conventional scan latches. The testing technique utilizes the clock input to the latches in the ICs for propagating data through the latches. The test technique includes coupling a drive 1 or drive 0 element to a logic element coupled to a general latch. The drive 1 or drive 0 scan element allows the general latch to be clocked by a clock signal such as a phi.1 clock signal or phi.2 clock signal.

US 5,428,622 to Kuban discloses a testing architecture with independent scan paths. The shift registers of one path 22a may receive test data that stimulates logic 28a,b,c on the IC to produce outputs received by shift registers on the other scan path 22b. This reduces the length of the scan path relative to a single scan path system.

US 5,430,735 to Sauerwald, et al. discloses a mode control register that controls the connection of a serial input 22 and serial output 24 to each other or further registers 32, 34, 36.

US 5,434,804 to Bock, et al., discloses a microprocessor provided with circuitry for receiving JTAG and ICE test control signals through JTAG test ports and for synchronizing the test signals to a chip clock signal. Test signals synchronized to an external JTAG device are processed internally by an ICE of the microprocessor chip once the test signals are synchronized

with the chip clock rate. To this end, the microprocessor is provided with a synchronizer which receives the chip clock signal, a JTAG control signal, and a JTAG reset signal, and outputs a synchronized control signal. The synchronizer includes an un-clocked SR flip-flop for sampling the JTAG control signal, and two or more DR flip-flops for synchronizing the JTAG control signal to the chip clock signal. The synchronizer may be configured to generate a control signal pulse or a control signal level. The synchronizer is protocol independent, i.e., the clock rate of the JTAG test commands is independent of the chip clock. Hence, no protocol is required to connect the JTAG test command signals to the ICE. In particular, the synchronizer includes an input stage configured for allowing the JTAG control signal to be much slower than the core clock signal or much faster than the core clock signal.

US 5,446,395 to Goto discloses test circuits for testing large scale integrated (LSI) circuits on a wafer. Test circuit 3 is formed on the wafer between two LSI circuits 21,22 and is connected to the circuits 21,22 by leads 4a-d. In Figure 4, test circuit 300 serves to test circuits 201-204.

US 5,448,576 to Russell discloses allowing selection of either a single bit register or a direct connection to be placed in the path between a device's TDI input and TDO output. The single bit register, in contrast to the bypass register, retains its current value at the point during data shifting that the bypass register is required to be set to zero. The single bit register of the preferred embodiment in contrast to the bypass register remains active in the TDI to TDO path during instruction scan operations as well as data scan operations. The direct connection minimizes the overall boundary scan chain bit length and also reduces dependency on device clocking for shift operations.

US 5,450,415 to Kamada discloses a boundary scan cell circuit for use in checking a wire, establishing a connection between the output pin of one IC and the input pin of the other IC, for stuck-at "0"/"1" faults. In an input boundary scan cell circuit in connection with the input pin, a

third selector, in response to a control signal, selects one of a signal from a logic signal input terminal and an XOR from an arithmetic unit thereby outputting a signal thus selected. The output of the third selector is latched by a first flip-flop. The arithmetic unit performs the XOR addition of the output of the first flip-flop and the value of a logic signal from the logic signal input terminal. The result of the XOR addition is scanned-out at a scan signal output terminal. This reduces the number of shift operation cycles required for scan-out of the test result thereby shortening the time taken for testing. In an output boundary scan cell circuit, test data is automatically logic-inverted, so that no shift operation cycles are necessary for scan-in of inverted test data, reducing the time taken for testing.

US 5,453,992 to Whetsel discloses selectable parallel execution of test operations. Corresponds to US 5,497,379.

US 5,457,400 to Ahmad, et al. discloses a test circuit in each integrated circuit on a wafer for testing the unsingulated integrated circuits. Corresponds to US 5,483,175.

US 5,469,473 to McClear, et al., discloses a bidirectional data transceiver circuit that automatically transfers data from a first bidirectional data port to a second bidirectional data port when new data is detected. The transceiver has a collision arbitration circuit that prevents the device from driving data onto a data port that is being driven externally. The transition detection circuitry of the transceiver is used to provide a input transition detection flag for an integrated circuit having standby or low power modes.

US 5,471,481 to Okumoto, et al., discloses a method of testing an electronic apparatus that eliminates a control signal line for setting an integrated circuit to a test mode. In each of the integrated circuits, a boundary scan control circuit discriminates a category code at the top of data inputted from a serial input terminal to control a pair of switching circuits. When the category

code represents a test mode, predetermined terminals of the switching circuits are selected so that input data are sent out to boundary scan cells. Fetching of parallel data from parallel input terminals and transfer to the boundary scan cells are performed at a time.

US 5,481,734 to Yoshida discloses a data processor having a 2N bits width data bus for a context switching function.

US 5,483,518 to Whetsel discloses an addressable shadow port and protocol for serial bus networks. The system provides for a serial bus master to select, communicate with, and deselect backplane boards so that high level test functions may be simultaneously executed and monitored. corresponds to US 5,581,541; US 5,617,420; US 5,640,521; US 5,875,353; and US 6,363,443.

US 5,488,614 to Shima discloses an integrated logic circuit provided with a plurality of test circuits for performing a Boundary-scan test. Each of the test circuits receives a clock signal, and comprises a first latch circuit for latching supplied data in response to a trailing edge of a clock signal, a second latch circuit for latching output data from the first latch circuit in response to the leading edge of the clock signal, and a third latch circuit for latching output data from the second latch circuit in response to the trailing edge of the clock signal. A pulse width of the clock signal is adjusted in accordance with a delay time of the clock signal.

US 5,488,728 to Dreyer discloses a microprocessor having a RUN/STOP pin for accessing an idle mode.

US 5,489,538 to Rostoker, et al. discloses a process of burn-in of semiconductor die of connecting die on a wafer and external current source, heating the wafer, and applying a common signal across the electrical connection to burn-in the die.

US 5,490,151 to Feger, et al. discloses a boundary scan cell having a shift flip-flop, an update flip-flop and a system flip-flop. An output from the system flip-flop is selectively applied to the input to the shift flip-flop.

US 5,491,666 to Sturges discloses an IEEE 1149.1 test standard boundary scan arrangement. Each of three different core logic circuits has a separate controller. See Figure 6. Corresponds to US 5,448,525.

US 5,491,699 to Scheuermann discloses a boundary scan cell that can be readily switched between tow-phase operation during testing and edge control during normal operation. The cell requires only one extra clock line.

US 5,526,310 to Dondale discloses maintaining the validity of the RAM output data after an address change occurs. The data is maintained valid until new data is written to the RAM.

US 5,526,365 to Whetsel discloses a boundary input/output serializer (BIOS) that eliminates the need of having to repetitively cycle through multiple 1149.1 data register scan operations to test a circuit. The BIOS, Figure 8, provides the internal timing and control for a DREG to input test patterns and to output test patterns from the boundary of sequential or combinational circuits during a single 1149.1 data register scan operation. Corresponds to US 5,606,566; US 5,687,312; US 6,006,343; and US 6,189,115.

US 5,532,174 to Corrigan discloses wafer level integrated circuit testing with a sacrificial metal layer. The metal layer is removed by etching before the die are separated.

US 5,534,786 to Kaneko, et al. discloses burn-in testing of dies from a wafer by recording the location of each die in a block of dies on the wafer.

US 5,541,935 to Waterson discloses an integrated circuit (IC) with multiple input-only, output-only and combination input/output terminals which can be functionally tested at both the IC and circuit board levels. The IC includes programmably-designated, internal test signal buses for allowing functional tests to be performed upon portions of the IC not normally accessible via its outside terminals. Programmably-controlled signal switches allow input and output test signals to be routed directly to and from those functional areas of the IC sought to be tested. Further included are a logic circuit for logically ANDing all of the input signals and programmably-controlled output signal buffers for selectively driving each output terminal to a logic zero, logic one or high impedance state, thereby allowing tests to be conducted to ensure that the various input and output terminals are not electrically shorted to one another or circuit ground.

US 5,544,174 to Abend discloses programmable boundary scan and I/O parameter ICs for testing ICs that have no internal boundary scan circuits.

US 5,548,781 to Huang discloses a data communication apparatus, such as a facsimile machine, and method for switching from a G3 and compatible mode to an ECM mode by inverting a protocol message signal.

US 5,550,843 to Yee discloses a scan chain for field programmable gate arrays with a programmable multiplexer for sequentially connecting columns of logic cells to enable the configuring of logic cell columns into one or more scan chains.

US 5,557,573 to McClure discloses testing in parallel all the integrated circuits, such as memory array parts, on a wafer by connecting only four probes to the wafer, power, ground, test mode 1 and test mode 2.

US 5,568,492 to Flint, et al. discloses a multichip module having plural integrated circuit die supports JTAG testing with plural registers in each die.

US 5,576,980 to Whetsel discloses a serializer circuit 40 for loading and shifting out digitized analog signals.

US 5,590,275 to Van Berkel, et al., discloses a testing method and associated arrangement for electronic circuitry that combines functional components that are interconnected by handshake channels. Various of such channels are now provided with an inbreaking junction and an outbreaking switch as a test component pair. The junction has two passive ports and one active port. The switch has one passive port and two active ports that are selected through a passive control port. In this way inbreaking into and outbreaking from the channel is rendered feasible. Now inbreaking is done on a first channel, and outbreaking on a second channel, so that thereby all components are tested that lie between the first channel's junction and the second channel's switch.

US 5,592,493 to Crouch et al. discloses a serial scan chain architecture for a data processing system. A controller 10 receives a serial data stream from STDI input and demultiples the data stream to one of the functional units 12, 14, 16, 18, 20, and 22. Each of the functional units is considered one scan chain and therefore the IC has six scan chains. In addition, a seventh scan chain couples all output flip-flops in each functional unit together between an output of the MUX 24 and the STDO output. Therefore a serial scan of a data stream can be done through one

functional unit, the multiplexer 24 and into the output flip-flops of each functional unit to make testing easier to set-up. The patent also discloses other scan chain cells and low power methods.

US 5,608,335 to Tailliet discloses forming a test circuit zone on a wafer and providing test selection circuits, such as decoders, in the zone for selecting testing of individual integrated circuits on the wafer.

US 5,608,736 to Bradford, et al. discloses a universal, programmable boundary scan driver/sensor circuit. Corresponds to US 5,726,999.

US 5,610,530 to Whetsel discloses a system for testing analog signals between ICs. See Figure 5.

US 5,610,826 to Whetsel discloses an analog signal monitor and method.

US 5,619,462 to McClure discloses a process of burn-in testing that exercises entire paths of buffers and monitors the current consumed by each die.

US 5,627,839 to Whetsel discloses serial scan path scan cell output latches using switches S1-S6 and bus holders BH. Corresponds to US 5,706,296.

US 5,640,404 to Satish discloses testing an integrated circuit when input/output pads of the integrated circuit are unconnected to any external device. For each of a subset of the unconnected input/output pads, a boundary scan register is provided. A test vector is scanned serially into the boundary scan registers. The test vector may then be applied to internal logic of the integrated circuit. While the test is in progress, the value contained within each boundary

scan register is applied to an associated input/output pad so that, as a result, the test vector is applied to the subset of the unconnected input/output pads.

US 5,648,661 to Rostoker, et al. discloses selecting unsingulated dies on a wafer by electronic selection circuits. Redundant conductive lines are provided to protect against "open" faults. Redundant electronic selection circuits may also be provided.

US 5,659,257 to Lu, et al. discloses a structure for measuring and testing discrete components interconnected with one or more integrated circuits on a mixed-signal circuit board. Each integrated circuit includes a test cell comprising a plurality of switches connected with a single on-chip bus which is in turn connected with a single circuit board bus. The structure permits a constant current to be supplied to the components over the single bus and voltage measurements to be made to determine the component values with a lower overhead in pins and board area.

US 5,659,773 to Huynh, et al. discloses a personal computer with an input and output island board 90, separate from the mother board carrying the microprocessor, also connected to an input/output connector panel 92 through communicating member 94. Corresponds to EP 0,486,146.

US 5,677,915 to Whetsel discloses a boundary input/output serializer (BIOS) that eliminates the need of having to repetitively cycle through multiple 1149.1 data register scan operations to test a circuit. The BIOS, Figure 8, provides the internal timing and control for a DREG to input test patterns and to output test patterns from the boundary of sequential or combinational circuits during a single 1149.1 data register scan operation. Figures 30-33 depict exemplary custom Boundary Input/Output Serializer circuits customized for use with known circuits under test.

US 5,685,004 to Bruce, et al. discloses a multi-level hierarchical bus architecture implemented with a multi-chip package and a modular shared-bus to provide high bandwidth. All IC components are mounted on standardized multi-chip packages. Each multi-chip package includes bus interface chips for providing communication from the integrated circuits to a board bus. One multi-chip package contains additional bus interface circuitry for providing communication from the board bus to a backplane bus. Corresponds to US 5,632,029.

US 5,687,179 to Whetsel discloses a memory access controller (MAC) 38 incorporated with test access port 12. The MAC provides for serial data to be written to and from a memory 36 without having to repetitively cycle through multiple shift operations. Corresponds to US 6,085,344; and US 6,158,035

US 5,701,307 to Whetsel discloses low overhead input and output boundary scan cells that include latching buffers. See Figures 4, 6, 8, and 10-16. Corresponds to US 5,859,860.

US 5,706,235 to Roohparvar, et al., discloses a memory circuit with a switch for selectively connecting an I/O pad directly to a non-volatile memory cell.

US 5,710,779 to Whetsel discloses a scan cell design including a bypass mode in which the scan input SI is connected directly to the scan output SO of the cell by a connection that bypasses the scan memory M1 of the cell.

US 5,715,171 to Mori et al. discloses a logical synthesizing device and method for designing semi-custom circuits and providing a net list to a test design section.

US 5,715,254 to Whetsel discloses a novel latchable output buffer (LOB) 51. An output boundary scan cell includes an output buffer structure connected between a shared capture/shift memory and an output terminal. The output buffer structure is responsive to initiation of a test mode of operation for latching at the output terminal functional test data from the shared capture/shift memory, and is operable to resolve voltage contention at the output terminal. Corresponds to US 5,732,091.

US 5,715,255 to Whetsel discloses functional input modules (FIM) that use latchable input buffers and functional output modules (FOM) that use latchable output buffers. See Figure 12. Corresponds to US 5,880,595; US 5,938,783; US 6,055,659; and US 6,378,095.

US 5,719,876 to Warren discloses a scan latch using a capture half-latch, a release half-latch, and an update half-latch.

US 5,719,878 to Yu, et al. discloses a system data transfer gate 22 and a scan data transfer gate 24 that minimize the setup time for data entering the data storage element 42.

US 5,744,949 to Whetsel discloses an analog test cell circuit.

US 5,760,643 to Whetsel discloses a process of testing integrated circuit die on a wafer. Selector circuits occur in the areas between the dies on the wafer. One selector circuit connects to one die and select between a functional mode and bypass mode for testing. Probe areas are formed on the periphery of the wafer and are connected to supply power and control to the dies and selector circuits. The testing occurs by selecting only one die in a particular row and column and maintaining the remaining dies in a standby mode. Corresponds to US 5,969,538; US 5,994,912; US 6,046,600; US 6,166,557; US 6,262,587; and US 6,326,801.

US 5,802,270 to Ko discloses parallel module testing with a single multiplexer 40.

US 5,805,792 to Swoboda et al. discloses emulation devices, systems and methods. A selecting circuit is responsive to bits in an emulation control register for coupling an address register and a data register to terminals of an IC ton enable serial scanning of the address and data registers.

US 5,825,785 to Barry, et al., discloses a serial input shift register built-in self test for embedded circuits. The built-in self test circuit receives a scan vector that describes the parameters of the embedded compiled macro that is to be tested. A state machine in the test circuit cycles through test vector generation, test vector application, data output scanning and compression for signature analysis. Parallel outputs of the compiled devices are serialized so that a serial shift register can be used for signature generation.

US 5,828,825 to Eskandari et al. discloses using the IEEE 1149.1 TAP to serially shift address, data and command information into respective fields of a memory access register located within a memory interface unit. This register acts as an interface between the TAP architecture and the embedded memories of the IC for reading and writing data to and from the specified memory locations.

US 5,841,670 to Swoboda discloses an emulation system with distributed control of clock domains.

US 5,841,791 to Hashizume discloses a plurality of bypass scan paths provided in series between an SI terminal and an SO terminal. In each of the bypass scan paths, a selection data propagation holding register and a mode data propagation holding register are not connected in series with a scan register and carry out no unnecessary shifting operations as in a conventional

scan path, but are arranged on a bypass path formed by a bypass line. As a result, the time period can be reduced for shifting in test data and shifting out test result data.

US 5,847,561 to Whetsel discloses an analog boundary scan cell (ABSC). See Figure 19.

US 5,862,152 to Handly et al. discloses a hierarchically managed boundary scan testable module and method. A JTAG module contains a master component 20 and any number of slave components 22. The boundary scan registers in the slave components form a boundary scan chain that originates and terminates at the master component.

US 5,872,908 to Whetsel discloses an analog boundary scan cell. See Figure 17.

US 5,883,524 to Whetsel discloses a latchable output buffer (LOB) used with circuit board testing with in-circuit testers (ICT). See Figure 19. Corresponds to US 5,852,354 and US 5,656,953.

US 5,884,023 to Swoboda, et al., discloses a method for testing a digital processor in which an 1149 test port is used to transfer trace data from the digital processor to a test host processor under control of a user definable program which executes in response to predetermined events on the digital processor.

US 5,887,004 to Walther discloses isolating scan paths in an IC to reduce the RC delay associated with the scan paths and reduce power consumption and reduce noise.

US 5,905,738 to Whetsel discloses a digital bus monitor (DBM) circuits 20,22. The DBM circuits observe data on address bus 14, data bus 16 and control bus 18 while the buses are in a functioning mode. The DBM circuits include memory and compare circuits. In response to a

matching condition, an event qualification module may perform a variety of tests on incoming data while the buses continue to operate at speed. Corresponds to US 6,131,171.

US 5,907,562 to Wrape et al. discloses a testable IC with reduced power dissipation. During functional operation, the data transitions in the scan path signals are disabled to reduce the power dissipation associated with driving the scan path signals.

US 5,958,072 to Jacobs, et al., discloses test-event hardware that can be repeatedly generated during a test procedure without repeated intervention by a test program. The hardware is located in the processor to memory bus interfaces of a system having multiprocessors.

US 5,968,191 to Thatcher, et al., discloses a method and apparatus for testing integrated circuit interconnects and measuring the value of passive component interconnecting the IC's. Each IC includes both analog and digital circuitry and is provided with a test access port and boundary scan architecture for selectively connecting components to an analog test bus and for testing for the integrity of interconnections. When connected with the test bus, a constant current is supplied to the component and the resulting voltage developed across the bus is used for identifying the value of the component. In a second embodiment each IC includes a pair of buses which permits measurement of the impedance of the switches connecting the components to the test bus.

US 5,968,192 to Kornachuk discloses a programmable memory test interface formed of a test controller 207. The controller 207 is accessible through plural programming pins, Figure 2C, to program the controller, as desired, for testing core memory.

US 6,000,051 to Nadeau-Dostie discloses performing the capture and update operations of an IEEE 1149.1 test procedure at the rate of the system clock.

US 6,028,983 to Jaber discloses providing a series of dedicated scan strings through which the IEEE 1149.1 test data selectively passes.

US 6,037,794 to Yamamoto, et al. discloses a probe wafer having bumps formed in mirror positions of bond pads of individual chips on a semiconductor wafer to be tested. The bumps come into contact with the bond pads and power and test signals are applied to the individual chips being tested.

US 6,073,254 to Whetsel discloses a TAP linking module 21,51 that permits plural TAPs TAP1-4 to be controlled and accessed from a test bus 13 via a single TAP interface 20. Corresponds to US 6,324,614.

US 6,115,763 to Douskey discloses a multi-core 60 chip providing external core access with a regular operation interface 54 and a test interface 58a comprising core interface units (CIU) 62 and a master interface unit (MIU) 58. Test or service bus 56 operates separate from operational bus 52 to allow testing during operation of the chip.

US 6,158,035 to Whetsel discloses a memory access controller (MAC) 38 incorporated with test access port 12. The MAC provides for serial data to be written to and from a memory 36 without having to repetitively cycle through multiple shift operations. Corresponds to US 5,687,179; and US 6,085,344

US 6,199,182 to Whetsel discloses probeless testing of pad buffers on a wafer to test input and output buffers and related peripheral circuits using boundary scan paths and three additional test bond pads. This provides testing without contacting the functional bond pads.

US 6,223,315 to Whetsel discloses an IP core design supporting a user-added scan register option. An IP core, with no internal boundary scan path, has a test access port 39 with an external register present (ERP) lead 37. An external scan register 25 encompasses the IP core and presents a signal on the ERP lead 37.

US 6,242,269 to Whetsel discloses parallel scan distributors 300,368 and collectors 344,412 for testing ICs. A scan distributor circuit 300 receives serial test data from a peripheral bond pad 302 and distributes it to each parallel scan path. A scan collector circuit 344 collects test data from the parallel scan paths and applies it to a peripheral bond pad 366. This enables more parallel scan paths of shorter length to connect to the functional circuits.

US 6,260,165 to Whetsel discloses that scan testing of plural target electrical circuits, such as circuits 1 through N, becomes accelerated by using the scan test response data output from one circuit, such as circuit 1, as the scan test stimulus data for another circuit, such as circuit 2. After reset, a scan path captures the output response data from the reset stimulus from all circuits. A tester then shifts the captured data only the length of the first circuit's scan path while loading the first circuit's scan path with new test stimulus data. The new response data from all the circuits then is captured in the scan path. This shift and capture cycle is repeated until the first circuit is tested. The first circuit is then disabled and any remaining stimulus data is applied to the second circuit. This process is repeated until all the circuits are tested. Corresponds to US 6,442,721.

US 6,286,121 to Osawa, et al., discloses that when a RAM (10) is not initialized, data signals captured from the data output portions (do[n]) may include undefined values, but these data signals are not transferred to a multiple input signature register (MISR) through the scan path (22). Transferred to the MISR are only the data signals (DI[n]) captured by the scan path (13). Accordingly, BIST can be applied to the combinational logic circuit (40) without requiring

initialization of the RAM (10) and without being affected by undefined value. Thus, BIST to the combinational logic circuit (40) can be normally achieved in a short period.

US 6,311,302 to Cassetti discloses an IC with multiple cores. Each core has multiple TAPs and an internal tap linking module (TLM). The TLM has an internal register adapted to store a decodable instruction and a supplemental storage circuit adapted to store a coded signal. A chip-level TLM communicates with a common IEEE JTAG interface and each of the multiple cores via the TLM register and the supplemental storage circuit.

US 6,324,614 to Whetsel corresponds to US 6,073,254.

US 6,324,662 to Haroun, et al. discloses a TAP Linking Module that includes an augmentation instruction shift register, used to access the TAP of one or more of plural embedded cores in an IC. The TAPs in the embedded cores remain unchanged. The augmentation shift register accepts a bit or bits augmenting a JTAG instruction to place the arrangement in a TAP scan mode or in a TAP Linking Module scan mode.

US 6,343,365 to Matsuzawa, et al. discloses dividing a scan path, in a large-scale integrated circuit, between an I/O scan path that is formed by a series connection between only flip-flops that are in a region near an I/O pin and between an internal scan path that is formed by a series connection between other flip-flops. A selector, controlled by a test mode signal, selects either all scan paths or only the I/O scan path.

US 6,446,230 to Chung discloses a compliance enabler working with non-compliant embedded boundary-scan cells to enable a Device Under Test (DUT) to function as an IEEE-standard-compliant part, thus allowing full utilization of existing test tool generation and operation of the IEEE standard. The enabler is provided separately from the boundary scan-cells

embedded in the core logic designs. The enabler includes a Test Access Port (TAP) controller and related decoding circuits to generate necessary compliance signals based on various conventional TAP controller variables and instruction functions. The embedded boundary-scan cells include an internal scan cell architecture.

US 6,457,148 to Yoshiba discloses testing an IC 2 with test units 4-1 and 4-2. To test a synchronous IC, pattern delay circuits 6-1 set a time delay corresponding to the latency set in the IC 2. The pattern delay circuits are connected between a pattern generator 10-2 and a logical comparator 9-2.

Foreign Patent Documents

EP 0,136,174 corresponds to US 4,618.956.

EP 0,148,403 A3 corresponds to US 4,680,539.

EP 0,190,494 A1 corresponds to US 4,740,970.

EP 0,195,164 A1 corresponds to 4,764,926.

EP 0,273,821 A2 corresponds to US 4,910,735.

EP 0,310,152 A2 (European patent application) to Wood discloses a synchronous test overlay circuit, Figure 3, interposed between blocks of logic to be tested.

EP 0,315,475 corresponds to 4,857,835.

EP 0,518,550 A2 discloses in-circuit testing of very large scale integrated devices having timing critical functions by use of controllable bi-directional driver/receivers associated with timing critical function pins.

EP 0,522,413 A2 discloses a boundary scan transmit cell having a three-state output buffer and logic circuitry for controlling the enabled or disabled state of the three-state buffer as a function of a scan input.

EP 0,604,032 A2 discloses scan cells or capture scan elements arranged in a pseudo master-slave configuration. The scan cells must be loaded twice because half the test data is lost when the data is propagated through the integrated circuit.

GB 2,220,272 A discloses testing a digital data storage circuit, in which the circuit includes two latch elements.

GB 2,266,965 A discloses boundary-scan testing for the reduction of testing-induced damage. The boundary-scan interconnect test is partitioned into four short-circuit sub-tests to reduce the potential for testing –induced damage. Open circuit testing is performed later.

JP 01-038,674 A discloses eliminating the need for an additional input terminal for testing by providing a test recognition circuit 9.

JP 01-043,773 (A) to Koji discloses testing a propagation delay to a flip-flop 104 by selecting the output of flip-flop 104 with a scan-address pin 112 to obtain the state of the flip-flop 104 output on scan-out pin 116.

JP 01-068,167 A discloses a fault detection processor. Signal checking means 2 detects the presence and absence of an error. Fault occurrence calculation means 3 calculates a fault occurrence frequency PF. Device test start means 4 starts a devices test circuit 9 as the frequency PF is a prescribed value or more.

JP 01-079,673 discloses circuitry with a lessened addition of testing terminals, by holding a written data of a RAM with an n-bit written data register while an address of the RAM is held with an m-bit address counter. When a scan pass mode selection terminal 80 for testing is in a 'written data register mode for testing', a scan clock is applied to a written data register 40 for testing (n-bit). When the terminal 80 is in an 'address count register mode', a scan clock is applied to an address count register 50 (m-bit) for testing. Moreover, when the terminal 80 is in a

'data select count register mode', a scan clock is applied to a data select count register 60 for testing. Then, when a shift mode signal is invalid, an output to the register 60 is outputted selectively to a scan out output terminal 100 to form a reading data of a RAM 180 thereby allowing a lessened addition of terminals for testing.

JP 01-110,274 (A) discloses a serial scan path between terminals 91 and 95, see Figure 1. Each of registers 100 (101-108) has three inputs: one serial input, a parallel input from the output of circuit block 10X and an input from the output of circuit block 10A. Shift registers 80A and 80D also are connected in the serial scan path.

JP 01-170,873 (A) discloses a set of serial registers, FFo-FFn, and gates, SEL, arranged to loop the data on the serial data output SOUT back into the serial registers.

JP 02-016,642 (A) discloses executing data processing and data diagnosis in parallel. Comparator 32 receives data signals from outputs B1-Bn of flip-flops 41-4n, which have shifting functions, and data signals A1-An from check data generation circuit 31. The comparison signal C from comparator 32 passes through AND gate 33.

JP 02-052,165 discloses counting triggers after a trigger condition and displaying the timing when a predetermined number is reached.

JP 02-062,984 A discloses an integrated circuit having a testing circuit that switches to a test mode without increasing the number of test pins.

JP 05-142,298 discloses facilitating a test by arbitrarily selecting a block to be tested from a plurality of blocks grouped by a scan path. A scan path length is changed to the necessary minimum.

JP 57-094,857 A apparently discloses a scan path 471-472 with three sets of latches 400-403, 410-413, and 430-433. Addresses are supplied to latches 400-403. The contents of the scratch pad memory is read to latches 430-433, which are then observed by shifting.

JP 57-209,546 (A) discloses flip-flops 2-1 through 2-n, storage registers 3A and 3B, multiplexers 4A, 4B and 4C, a comparison condition setting flip-flop 5 and a comparison circuit 6. Storage registers 3A and 3B contain scanning addresses loaded externally. Multiplexers 4A and 4B selectively output the contents of the flip-flops 2-1 through 2-n according to the addresses stored in them. Multiplexer 4C outputs the contents of the selected flip-flop according to the addresses present on address line l.

JP 58-155,599 to Wada, et al. discloses a memory testing circuit.

JP 58-191,021 A discloses detecting a fault in comparator 3 by comparing the received input interface 2 with a standard input stored in memory 1.

JP 59-210,382 (A) discloses testing an LSI circuit with scan-in flip-flops 23aa-23ag and scan-out flip-flops 23ba-23br. Testing device 1 provides an address decoded in decoder 25 to select one scan-in and one scan-out flip-flop. The outputs of the flip-flops are connected through an OR gate 26 to a testing device, which compares the outputs to decide whether the LSI is normal.

JP 60-140,834 discloses that the comparison circuit 2 compares the outputs of the 4 bit register 1 with the expected data outputs of register 3.

JP 60-252,958 discloses scan flip-flops 35a-35c in each input/output circuit unit 31. Necessary data are transmitted in series using a small number of connecting lines distributed by a decoder 34.

JP 60-262,073 discloses monitoring the operation of digital signal processor 1 by simulation processor. Input data on input signal line IL is stored in memory 6. Output from the digital signal processor 1 is stored in memory 7. Simulation processor 8 processes the data from memory 6 and the output of processor 8 is compared in comparator 3 with the data stored in memory 7. Non-coincidence causes a signal on terminal 5.

JP 62-031,447 A discloses monitoring and recording data on a data bus independent of a computer to be monitored. The monitored data is compared with other data to determine stop conditions.

JP 62-228,177 (A) discloses circuits 11-13 that capture the logical states on terminals 1-4. The contents of circuits 11-13 can be clocked out on terminal 23 by placing a low on terminal 4.

JP 62-280,663 discloses logic circuit 110. Fault detection circuits 121-12n detect faults in logic circuit 110 at particular locations. Flip-flops 141-14n save the detected fault state through selectors 131-13n. Logic circuit 150 receives the outputs of flip-flops 141-14n and produces a fault signal at terminal C.

JP 63-073,169 (A) discloses reducing by one pin the number of pins used for normal and test operation. Pin 6 is multiplexer for both data and test.

JP 63-188,783 A discloses a logic analyzer. A detector 10 detects a prescribed logic relation among plural binary inputs. Time width detection part 20 determines whether the prescribed logic relation occurs for a prescribed time. Selection part 30 selects a prescribed input signal to be analyzed.

JP 63-213,014 A discloses shift path control means 100 passing an instruction to clock transmission instruction means 200 that controls transmission of a clock signal to each of 1st shift path logical units 400,410, 2nd shift path logical units 420,430,440, and 3rd shift path logical unit 450.

JP 63-310,046 A discloses a test auxiliary circuit. The circuit reduces a serial shift operation to read out response data of a circuit to be tested by latching data at an input terminal to a latch circuit only when the data at a parallel input terminal differs from expected value data.

JP 64-006,572 discloses in Figure 1 an Exclusive-OR gate 8 receiving the outputs of input shift registers 2 and output shift registers 5.

Other Documents

The Adshead paper, June, 1998, discloses JTAG accelerating the debugging process. This paper specifically addresses the difficulties, including timing, in debugging an integrated circuit having three processors communicating with one another through a mailbox.

The Avra paper discloses a test and maintenance control block that receives commands serially over an ETM-BUS to control chip level test and maintenance features such as chip initialization, serial scan, debug and built-in self-test operations.

The Bhavsár, et al. paper (1981) discloses self testing by polynomial division in feed back shift registers for test vector generation and response evaluation.

The Bhavsar paper (1990) discloses a modified boundary-scan cell with a second observation tap taken from the output of the output buffer driver via a dedicated receiver. The output of the output buffer driver passes through a receiver circuit to a third input of the input multiplexer of the cell. The input multiplexer also receives a test data input and an operational data input.

The Bhavsar paper (1991) discloses extending the protocol of 1149.1 so it can be used to access an interface circuit residing between the backplane and board level 1149.1 buses. The interface circuit responds to 1149.1 protocol transmitted over the backplane bus to load an address. If the address matches the address of the interface circuit, the interface circuit is connected to the backplane. After the interface circuit is connected to the backplane, additional 1149.1 protocol is input to the interface circuit to connect the backplane and board level 1149.1 buses. Following this connection procedure, the board level 1149.1 bus can be controlled by the backplane 1149.1 bus.

This approach does not allow selecting one board, then selecting another board without first resetting the backplane and board level 1149.1 buses, by transitioning them into their test logic reset (TLRST) states. Entering the TLRST state causes test conditions setup in the ICs of a previously selected board to be lost due to the test reset action of the 1149.1 bus on the test access ports (TAPs) of the ICs.

Also, it is often desirable to select and initiate self-tests in a selected group of backplane boards. However, since the this approach requires resetting the 1149.1 bus each time a new board is selected, it is impossible to self-test more than one board at a time, because resetting the bus aborts any previously initiated self-test.

The Blair, et al. paper discloses a token ring LAN chip includes self-test features including internal and boundary scan chains. See Figure 9.

The Breuer, et al. paper discloses a module test and maintenance controller (MMC) for testing chips. The controller tests every chip in a module by an ETM-BUS or a Boundary Scan bus. The MMC requires either a RISC-type processor or DMA controller.

The Bruce paper discloses problems and solutions that arose in implementing IEEE 1149.1 testing in Motorola VLSI CMOS microprocessors.

The Carbine, et al. paper, November, 1997, discloses the design for test (DFT) and silicon debug features of the Pentium® Pro processor, and its production test development methodology. The DFT features include a JTAG test access port and over 2000 scan nodes.

The Colwell et al. paper discloses an Intel processor with testability features built into the design, including test registers, mode bits to provide specific logic access and the use of serial scan

chains. The scan chains provide observability of virtually all important signals within the design with no speed impact.

The Dervisoglu paper (1988) discloses an architecture for implementing scan technology for test and debug in a sate-of-the-art workstation.

The Dervisoglu paper (1992) discloses the differences between the IEEE 1149.1 and 1149.2 standards. The 1149.2 boundary-scan register cells can be shared with the core logic of the component and are not required to have separate serial-shift and parallel-update stages. The 1149.2 standard uses a direct, parallel access method to enable the different test modes. The component must have a minimum of two dedicated select test mode inputs, to select one of several possible test and/or operating modes. The 1149.2 standard should allow the use of software tools developed the support the 1149.1 standard.

The Dervisoglu paper (1998) proposes extensions to the IEEE 1149.1 Boundary Scan structures, including shared I/O-Cells and other proprietary features. These include shared I/O cells for performance, shared serial shift stages, the absence of an update stage, separate public and private operations, and separate compliant and non-compliant test modes.

The El-ziq, et al. paper discloses a mixed-mode built-in self-test technique using scan path and signature analysis.

The ETM-Bus Specification paper discloses the performance requirements for a particular test bus.

The George paper discloses loading an SRAM-based FPGA with the 1149.1 standard boundary-scan test logic and then re-program it for normal operation when the diagnostics are complete.

The Gerstendorfer, et al. paper discloses reducing power consumption during testing by masking the scan path activity during shifting and inserting additional logic to suppress random patterns that do not contribute to increase the fault coverage.

The Gott paper, February, 1998, describes debugging embedded software. A JTAG port permits processor resources to be loaded and examined under control of a JTAG driver on the host computer.

The Haedtke, et al. paper discloses multilevel self-test for the factory and field. Figure 4 depicts a simplified bi-directional boundary scan I/O cell.

The Hahn, et al. paper discloses VLSI testing by on-chip error detection with scanned and expected data being latched in respective latches. The outputs of the two latches connect to an exclusive OR gate to determine any error.

The Heatherington paper discloses moving from an automatic test generation tool to a STUMPS logic BIST methodology in testing ASIC integrated circuits with multi-clock designs and 200K to 800K gates.

The Hudson, et al. paper (1987) discloses parallel self test with pseudo-random test patterns.

The Hudson, et al., paper (1988) discloses integrating BIST and boundary scan on a board.

The Hunter, et al., paper discloses testing of the G2 PowerPC 603e microprocessor from Motorola.

The IBM Technical Disclosure Bulletin (1985) discloses a bi-directional double latch that can be used in Level Sensitive Scan Designs.

The IBM Technical Disclosure Bulletin (1988) discloses a self-contained performance monitor for a personal computer. The monitor interrogates the PC I/O for 2 programmable events and 1 external event. When an event occurs, a timer value, the PC data bus, and identification information are captured and automatically gated into a battery-back-up RAM. The RAM is read through a register 60 connected to a register bus.

The IBM Technical Disclosure Bulletin, August, 1989, discloses a test bus architecture.

The IEEE P1149.2-D2.5 paper discloses a proposed standard similar to IEEE 1149.1. This new standard provides that boundary-scan register cells can be shared with the core logic of the component and are not required to have separate serial-shift and parallel-update stages. The 1149.2 standard uses a direct, parallel access method to enable the different test modes. The component must have a minimum of two dedicated select test mode inputs, to select one of several possible test and/or operating modes. The 1149.2 standard should allow the use of software tools developed the support the 1149.1 standard.

The Intel 80386 Programmer's Manual discloses the debugging features of the 80386 architecture and the registers used for debugging. The principal debugging support takes the form of debug registers. The debug registers support both instruction breakpoints and data breakpoints. A reserved debug interrupt vector permits the processor to automatically invoke a debugger task or procedure when an event occurs that is of interest to the debugger. The debug registers are accessed by variants of the MOV instruction.

The Intel Microprocessor and Peripheral Handbook discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the

page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

The Intel Microprocessor and Peripheral Handbook, Section 2.11.2 TLB Testing, also discloses that there are two TLB (Translation Lookaside Buffer) testing operations. One is to write entries into the TLB. The other is to perform TLB lookups. C: is the command bit. A "0" written into this bit causes an immediate write into the TLB entry. A "1" written into this bit causes an immediate TLB lookup.

The Intel386™ DX Microprocessor data sheet discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

In Section 2.11.2 TLB Testing, when testing, the Translation Lookaside Buffer must be turned off (PG=0 in CRO) to enable the TLB testing hardware and avoid interference with the test data being written to the TLB. There are two TLB testing operations: 1) write entries into the TLB, and 2) perform TLB lookups. Two Test Registers, shown in Figure 2-12, are provided for the purpose of testing. TR6 is the "test command register", and TR7 is the "test data register". Figure 2-12 depicts the fields within the registers.

C: is the command bit. For a write into TR6 to cause an immediate write into the TLB entry, write a 0 into this bit. For a write into TR6 to cause an immediate TLB lookup, write a 1 to this bit.

The Jarwala paper discloses testing of mixed analog and digital circuits. The 1149.1 standard is used for testing the digital circuit blocks. The analog circuits are partitioned into sub-blocks. Structured access is provided to the analog sub-blocks via a DFT framework.

The Joint Test Action Group paper, January, 1988, discloses an early version of the standard for a boundary scan test architecture.

The Jungert, et al., paper discloses bus drivers and latches with JTAG test port products made by Texas Instruments.

The Kuban paper discloses a built-in self-test of a Motorola microprocessor having a serial architecture. The self-test is based on a ROM-driven signature analysis technique. The resulting signature is output from the microprocessor for external examination of the signature.

Referring to Figure 9 and the description on page 39, right-hand column, the operating mode of the MC6804P2 is controlled by RESET, MDS, PA7, and PA6. When RESET is brought high, the levels on the MDS, PA7, and PA6 pins are sampled, and the appropriate mode is selected. The two test modes are invoked by a high on the MDS and PA7 pins. The functional test is then entered if the PA6 pin is low; otherwise, a high on PA6 invokes the ROM verify test. The self-test fixture provides a good/bad indicator for the ROM verify test.

The Laurent paper discloses implementing a boundary scan path and an internal scan path in VLSI circuits. Figures 2 and 3 depict respective input and output buffers.

The Lee paper discloses testing of analog and mixed signal devices. A serial scan chain is used to scan 1s and 0s to selected flip-flops. The outputs of the flip-flops control bi-directional analog switches. The analog switches isolate partitioned parts of the analog circuits and connected

selected parts of the analog circuits to external test pads. The analog state of the selected analog partition can be observed and tested.

The Lien paper discloses a Module test and Maintenance Controller (MMC) that can test every chip on a JTAG boundary scan bus and control more than one test bus. The MMC includes a test-channel that, once initialized by the MMC processor, controls testing across a specific test bus.

The Lofstrom (1996) paper discloses measuring analog waveforms and delays using a simple extension of the IEEE 1149.x standards. Early capture samples data on a falling edge of TMS during the Update-DR State.

The Lofstrom (A Demonstration IC) paper discloses an 1149.4 mixed signal boundary scan standard demonstrated with a CMOS integrated circuit. The 1149.4 standard provides simple shorts and open testing. The standard also provides two probe parametric testing in which all pins may be connected to one or both of the on-chip global wires AB1 and AB2 for connection to external test pins AT1 and AT2.

The Maierhofer paper discloses a hierarchical self-test concept based on the JTAG standard. The concept is based on a hierarchy of controllers, which control the self-test on each level.

The Marinissen paper discloses the IEEE P1500 Core Test Standard.

The Marlett, et al. paper discloses a RISP methodology for testing integrated circuits.

The Maunder et al. paper discloses an industry-standard boundary-scan framework for merchant and custom integrated circuits. The boundary-scan path provides for external, internal and self-testing of integrated circuits through shift register-latch scan-cells located at the bond pads

of the integrated circuit. Figure 9 depicts one possible implementation of a scan-cell complying with JTAG requirements. The paper also discloses testing analog signals.

The Mixed Signal Working Group paper discloses a proposed standard P1149.4 for testing mixed signal integrated circuits.

The Ohletz, et al. paper discloses investigating the overhead for different scan designs and self-testing designs.

The Ohsawa, et al. paper discloses a 4 Mbit CMOS DRAM with built-in self-test. A board carrying 64 4 Mbit x 1 DRAMs provides for simultaneous testing of all DRAMs in one row.

The Paraskeva, et al. paper discloses a new structured test register for VLSI self-test. See Figure 1.

The Parker (1989) paper discloses the impact of boundary scan on board test.

The Parker (1993) paper discloses structure and metrology for an analog testability bus.

The Pradhan et al paper discloses a circular BIST technique to perform a random test of sequential logic. Additional deterministic tests are presented to the circuit under test by configuring the circular path as a partial scan chain.

The Russell paper discloses the JTAG proposal and its impact on automatic testing. Figure 2 depicts an input pin cell and Figure 3 depicts an output pin cell.

The Sabo paper discloses the costs of not designing for test.

The Sasidhar, et al. paper, "Optimal Multiple Chain Relay ...", discloses an optimal scheme for testing multi-chip modules on large area substrates using the IEEE 1149.1 boundary scan standard.

The Sasidhar, et al. paper, "Relay Propagation Scheme...", discloses a parallel and pipelined relay propagation scheme for testing multi-chip modules. The scheme re-uses test vector sets for multiple multi-chip modules without the need to re-apply them through physical probing or to serialize the test application.

The Sellers, et al. book extract illustrates four ways to design an error correction circuit in Figures 12.2a-12.2d.

The Sharp paper, June, 1998, discloses using JTAG emulation systems to explore embedded cores. The paper uses a 5-pin JTAG interface and a test access port,that are traditionally used for functional testing, for in-circuit-emulation. Additional functionality can be achieved by adding further macrocells to a core circuit.

The Sunter paper (1995) discloses a low cost 100 MHz analog test bus.

The Sunter paper (1996) describes a P1149.4 standard and a cost/benefit analysis of using this standard.

The Texas Instruments data book provides a product review of a Test Bus Controller integrated circuit. This test bus controller provides control of six parallel target scan paths under the IEEE 1149.1 test standard.

The van Riessen, et al. paper discloses integration of the boundary scan standard with the built-in self test approach. The built-in self test uses a macroprocessor, see Figure 7 to produce a test signature.

The Wagner paper discloses interconnect testing with boundary scan. Figure 4 depicts a boundary scan bit-slice.

The Wang, et al. (1986) paper discloses a concurrent built-in logic block observer combines the scan and BILBO techniques.

The Wang, et al. (1989) paper discloses using a JTAG boundary scan bus with pseudorandom patterns from a cellular automaton to locate defective chips and walking sequences to locate bad interconnects.

The Whetsel (January, 1988) paper discloses an overview of the JTAG IC test architecture. The disclosed architecture is readily expandable to accommodate boundary scan and other IC test structures such as built-in self test (BIST) and internal core scan design. Figure 8 depicts a boundary register bit.

The Whetsel (July, 1988) paper discloses a standard test bus and boundary scan architecture used by Texas Instruments Incorporated in its implementation of the JTAG architecture. The disclosure covers the scan path, a scan cell, a test access port and instruction and data registers, and state diagrams.

The Whetsel (October, 1988) paper discloses a proposed standard test bus and boundary scan architecture from the Joint Test Action Group.

The Whetsel (1989) paper discloses a scan path selector (SPS) integrated circuit that provides for coupling and decoupling board level secondary scan paths to a primary scan path. See Figure 2. In connection with Figure 3, the test board controller TBC must have a TMS lead for each scan path to be selected. The SPS circuit provides for the same number of scan paths with one TMS lead. Figure 4 depicts the SPS including the usual 1149.1 tap and register circuits. Figure 5 depicts a digital bus monitor (DBM) circuit used to monitor data, address and control digital signal paths.

The Whetsel (October, 1991) paper discloses a data bus manager (DBM) circuit, embedded in the circuits to be tested, that provides for at speed testing of the circuits. The DBM is enabled via serial input from the 1149.1 test bus and synchronizes with the functional circuit. The DBM performs data trace and/or data compaction on the high speed flow between the functional circuits. The trace data or signature can be accessed via the 1149.1 test bus for processing. The DBM includes an event qualification module and a comparator.

The Whetsel (February, 1993) paper discloses an introduction to the IEEE 1149.1 standard.

The Whetsel (1995) paper discloses improved 2-state and 3-state output boundary scan cells and an improved input boundary scan cell. The improved cells generally use switches instead of multiplexers and also provide weak feed back buffers at the output or input buffers.

The Whetsel (November, 1997) paper discloses accessing embedded cores in an IC with a TAP Linking Module. The TAP Linking Module uses enable and select leads to access the TAP in each embedded core on the IC. This requires the TAP in each core to be modified to operate with the new enable and select leads.

The Whetsel (September, 1999) paper discloses using addressable test ports to test embedded cores. Each core includes an addressable test port that can be individually addressed to test the addressed core.

The Zorian, et al. paper discloses using a Test Access Port to control and repair the microprocessor as well as to control and observe key control and data values.

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		TI-30726	09/803,698
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		Whetsel.	
		FILING DATE	GROUP
		3/9/2001	2133

LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

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EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (REV. 7-80)

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		4,534,028	8/6/1985	Trischler	371	25	12/1/1983
		4,553,090	11/12/1985	Hatano, et al.	324	73 AT	7/23/1980
		4,575,674	3/11/1986	Bass, et al.	324	73 R	7/1/1983
		4,577,318	3/18/1986	Whitacre, et al.	371	1	11/14/1983
		4,587,609	5/1/1986	Boudreau, et al.	395	726	7/1/1983
		4,594,711	6/10/1986	Thatte	371	25	11/10/1983
		4,597,042	6/24/1986	d'Angeac	364	200	9/13/1983
		4,597,080	6/24/1986	Thatte, et al.	371	25	11/14/1983
		4,598,401	7/1/1986	Whelan	371	25	6/25/1984
		4,601,034	7/15/1986	Sridhar	371	25	3/30/1984
		4,602,210	7/22/1986	Fasang, et al.	324	73	12/28/1984
		4,612,499	9/16/1986	Andresen, et al.	324	73 R	11/7/1983
		4,615,029	9/30/1986	Hu, et al.	370	89	12/3/1984
		4,618,956	10/21/1986	Horst	371	68	9/29/1983
		4,621,363	11/4/1986	Blum	371	25	12/6/1984
		4,627,018	12/1/1986	Trost, et al.	395	476	9/8/1983
		4,628,511	12/9/1986	Stitzlein, et al.	371	22	2/25/1982
		4,635,193	1/6/1987	Moyer, et al.	364	200	6/27/1984
		4,635,261	1/6/1987	Anderson, et al.	371	25	1/26/1985
		4,638,313	1/20/1987	Sherwood, et al.	340	825.52	11/8/1984

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,642,561	2/10/1987	Groves, et al.	324	73 R	6/13/1983
		4,646,298	2/1/1987	Laws, et al.	371	16	5/1/1984
		4,646,299	2/24/1987	Schinabeck, et al.	371	20	8/1/1983
		4,651,088	3/17/1987	Sawada	324	73R	5/6/1985
		4,669,061	5/26/1987	Bhavsar	365	154	12/21/1984
		4,672,307	6/9/1987	Breuer, et al.	324	73 R	12/20/1985
		4,674,089	6/16/1987	Poret, et al.	371	25	4/16/1985
		4,679,192	7/1/1987	Vanbrabant	340	825.52	1/24/1986
		4,680,539	7/14/1987	Tsai	324	73	12/30/1983
		4,680,733	7/14/1987	Duforestel	364	900	10/29/1984
		4,683,569	7/28/1987	Rubin	371	25	10/21/1985
		4,687,988	8/18/1987	Eichelberger, et al.	324	73 AT	6/24/1985
		4,694,293	9/15/1987	Sugiyama, et al.	340	825.68	9/16/1985
		4,698,588	10/6/1987	Hwang, et al.	324	73 R	10/23/1985
		4,701,916	10/20/1987	Naven, et al.	371	15	3/17/1986
		4,701,920	10/20/1987	Resnick, et al.	371	25	11/8/1985
		4,701,921	10/20/1987	Powell, et al.	371	25	10/23/1985
		4,710,931	12/1/1987	Bellay, et al.	371	25	10/23/1985
		4,710,932	12/1/1987	Hiroshi	371	25	1/15/1986
		4,710,933	12/1/1987	Powell, et al.	371	25	10/23/1985
		4,734,921	3/29/1988	Giangano, et al.	377	72	11/25/1986
		4,740,970	4/26/1988	Burrows, et al.	371	15	12/11/1985
		4,743,841	5/10/1988	Takeuchi	324	73 R	5/20/1985
		4,745,355	5/17/1988	Eichelberger, et al.	324	73 R	6/24/1985
		4,752,929	6/21/1988	Kantz, et al.	371	21	3/25/1986
		4,759,019	7/19/1988	Bentley, et al.	371	3	7/10/1986
		4,763,066	8/9/1988	Yeung, et al.	324	73R	7/23/1986
		4,764,926	8/16/1988	Knight, et al.	371	25	12/11/1985
		4,777,616	10/11/1988	Moore, et al.	364	900	5/12/1986
		4,783,785	11/8/1988	Hanta	371	25	1/5/1987
		4,788,683	11/29/1988	Hester, et al.	371	20	1/14/1986
		4,791,358	12/13/1988	Sauerwald, et al.	324	73 R	9/2/1986
		4,799,004	1/17/1989	Mori	324	73 R	1/25/1988
		4,799,052	1/1/1989	Near, et al.	340	825.52	1/13/1986

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,800,418	1/24/1989	Natsui	357	68	9/6/1984
		4,801,870	1/31/1989	Eichelberger, et al.	324	73R	6/24/1985
		4,802,163	1/31/1989	Hirabayshi	371	15	12/29/1986
		4,808,844	2/28/1989	Ozaki, et al.	307	243	4/17/1986
		4,811,299	3/7/1989	Miyazawa, et al.	365	201	4/22/1987
		4,812,678	3/14/1989	Abe	307	443	3/23/1987
		4,817,093	3/28/1989	Jacobs, et al.	371	25	6/18/1987
		4,819,234	4/4/1989	Huber	371	19	5/1/1987
		4,821,269	4/11/1989	Jackson, et al.	371	16	10/23/1986
		4,825,439	4/25/1989	Sakashita, et al.	371	15	8/18/1987
		4,833,395	5/23/1989	Sasaki, et al.	324	73 R	10/23/1987
		4,833,676	5/23/1989	Koo	371	15	7/30/1987
		4,855,954	8/8/1989	Turner, et al.	365	185	3/4/1985
		4,857,835	8/15/1989	Whetsel	324	73	11/5/1987
		4,860,288	8/22/1989	Teske, et al.	371	1	10/23/1987
		4,860,290	8/22/1989	Daniels, et al.	371	25	6/2/1987
		4,862,071	8/29/1989	Sato, et al.	324	73 R	11/18/1988
		4,862,072	8/29/1989	Harris, et al.	324	73 R	9/8/1988
		4,864,570	9/5/1989	Savaglio, et al.	371	22.4	6/29/1987
		4,864,579	9/5/1989	Kishida, et al.	371	22.3	8/3/1987
		4,866,508	9/12/1989	Eichelberger, et al.	357	74	9/26/1986
		4,870,345	9/26/1989	Tomioka, et al.	371	22.3	8/3/1987
		4,872,169	10/3/1989	Whetsel	371	22.3	3/6/1987
		4,875,003	10/17/1989	Burke	324	73 R	2/21/1989
		4,878,168	10/31/1989	Johnson, et al.	364	200	10/29/1986
		4,879,717	11/7/1989	Sauerwald, et al.	371	22.3	9/2/1986
		4,887,262	12/12/1989	van Veldhuizen	370	85.1	3/15/1988
		4,887,267	12/12/1989	Kanuma	371	22.3	12/28/1987
		4,893,072	1/9/1990	Matsumoto	371	223	6/22/1988
		4,894,830	1/16/1990	Kawai	371	22.3	1/19/1988
		4,896,262	1/23/1990	Wayama, et al.	364	200	2/22/1985
		4,897,842	1/30/1990	Herz, et al.	371	22.4	11/5/1987
		4,899,273	2/6/1990	Omoda, et al.	364	200	12/10/1986
		4,903,266	2/20/1990	Hack	371	21.2	4/29/1988
		4,907,230	3/6/1990	Heller, et al.	371	22.1	2/29/1988

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,910,735	3/20/1990	Yamashita	371	22.4	12/17/1987
		4,912,633	3/27/1990	Schweizer, et al	364	200	10/24/1988
		4,912,709	3/27/1990	Teske, et al.	371	22.1	10/23/1987
		4,918,379	4/17/1990	Jongepier	324	73.1	8/31/1988
		4,924,468	5/8/1990	Horak, et al.	371	22.1	11/16/1988
		4,926,425	5/15/1990	Hedtke, et al.	371	22.6	6/9/1988
		4,929,889	5/29/1990	Seiler, et al.	371	22.3	6/13/1988
		4,930,216	6/5/1990	Nelson	29	854	3/10/1989
		4,931,722	6/5/1990	Stoica	371	22.5	11/7/1985
		4,931,723	6/5/1990	Jeffrey, et al.	371	22.3	12/18/1985
		4,935,868	6/1/1990	DuLac	364	200	11/28/1988
		4,937,826	6/26/1990	Gheewala, et al.	371	22.1	9/9/1988
		4,943,966	7/24/1990	Giunta, et al.	371	11.1	4/8/1988
		4,945,536	7/31/1990	Hancu	371	22.3	9/9/1988
		4,947,106	8/7/1990	Chism	324	73.1	3/31/1988
		4,947,357	8/7/1990	Stewart, et al.	371	22.3	2/24/1988
		4,956,602	9/11/1990	Parrish	324	158 R	2/14/1989
		4,961,053	10/2/1990	Krug	324	158 R	7/24/1985
		4,969,121	11/6/1990	Chan, et al.	364	900	3/2/1987
		4,974,192	11/27/1990	Face, et al	364	900	7/23/1987
		4,974,226	11/27/1990	Fujimori, et al.	371	22.3	9/22/1988
		4,989,209	1/29/1991	Littlebury, et al.	371	22.1	3/24/1989
		4,992,985	2/12/1991	Miyazawa, et al.	365	201	4/22/1987
		5,001,713	3/19/1991	Whetsel	371	22.3	2/8/1989
		5,008,618	4/16/1991	Van Der Star	324	158 R	1/23/1990
		5,008,885	4/16/1991	Huang, et al.	371	3	12/29/1988
		5,012,185	4/30/1991	Ohfuji	324	158 R	10/16/1989
		5,014,186	5/1/1991	Chisholm	395	850	8/1/1986
		5,023,872	6/11/1991	Annamalai	371	5.1	3/25/1988
		5,042,005	8/20/1991	Miller, et al.	364	900	8/19/1988
		5,048,021	9/10/1991	Jarwala, et al.	371	22.3	8/28/1989
		5,051,996	9/24/1991	Bergeson, et al.	371	22.4	3/27/1989
		5,053,949	10/1/1991	Allison, et al.	364	200	4/3/1989
		5,054,024	10/1/1991	Whetsel	371	22.3	8/9/1989

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		5,056,093	10/8/1991	Whetsel	371	22.3	8/9/1989
		5,056,094	10/8/1991	Whetsel	371	25.1	6/9/1989
		5,070,296	12/3/1991	Priebe	324	73.1	6/22/1990
		5,070,297	12/3/1991	Kwon, et al.	324	158 P	6/4/1990
		5,077,740	12/31/1991	Kanuma	371	22.3	1/30/1989
		5,084,814	1/28/1992	Vaglica, et al.	395	325	10/30/1987
		5,084,874	1/28/1992	Whetsel	371	22.3	9/7/1988
		5,090,015	2/18/1992	Dabbish, et al.	371	22.5	2/6/1989
		5,090,035	2/18/1992	Murase	377	72	1/22/1991
		5,107,148	4/21/1992	Millman	307	473	4/12/1991
		5,107,489	4/1/1992	Brown, et al.	370	58.2	10/30/1989
		5,109,190	4/28/1992	Sahashita, et al.	324	158 R	2/22/1991
		5,109,383	4/28/1992	Chujo	371	22.3	9/1/1989
		5,115,191	5/19/1992	Yoshimori	324	158 R	6/11/1991
		5,115,435	5/1/1992	Langford, II, et al.	371	22.1	10/19/1989
		5,126,286	6/30/1992	Chance	437	203	10/5/1990
		5,128,664	7/1/1992	Bishop	340	825.52	5/5/1986
		5,130,988	7/1/1992	Wilcox, et al.	371	22.3	9/17/1990
		5,132,635	7/1/1992	Kennedy	371	22.3	3/5/1991
		5,133,062	7/1/1992	Joshi, et al.	395	500	3/6/1986
		5,134,314	7/28/1992	Wehrmacher	307	443	12/18/1990
		5,150,044	9/1/1992	Hashizume, et al.	324	158 R	3/22/1991
		5,150,047	9/22/1992	Saito, et al.	324	158 R	7/17/1990
		5,155,432	10/13/1992	Mahoney	324	158 R	10/7/1987
		5,159,465	10/1/1992	Maemura, et al.	326	73	10/5/1988
		5,161,160	11/3/1992	Yaguchi, et al.	371	22.3	2/1/1990
		5,165,022	11/1/1992	Erhard, et al.	395	275	11/23/1989
		5,167,020	11/24/1992	Kahn, et al.	395	250	5/25/1989
		5,170,398	12/8/1992	Fujieda, et al.	371	27	7/18/1990
		5,172,377	12/1/1992	Robinson, et al.	371	22.3	9/7/1990
		5,173,906	12/22/1992	Dreibelbis, et al.	371	22.5	8/31/1990
		5,175,447	12/29/1992	Kawasaki, et al.	307	480	4/19/1991
		5,187,795	2/1/1993	Balmforth, et al.	395	800	1/27/1989
		5,191,653	3/1/1993	Banks, et al.	395	275	12/28/1990
		5,202,625	4/13/1993	Farwell	324	158 R	7/3/1991

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		5,206,545	4/27/1993	Huang	307	443	2/5/1991
		5,210,759	5/11/1993	DeWitt, et al.	371	22.3	11/19/1990
		5,214,760	5/1/1993	Hammond, et al.	395	250	8/26/1988
		5,214,774	5/1/1993	Welsch, et al.	455	11.1	7/30/1990
		5,218,702	6/1/1993	Kirtland	395	298	7/6/1988
		5,241,265	8/31/1993	McDonnell, et al.	324	158 R	3/26/1992
		5,241,266	8/31/1993	Ahmad, et al.	324	158 R	4/10/1992
		5,252,917	10/12/1993	Kadowaki	324	158 R	4/24/1991
		5,254,942	10/19/1993	D'Souza, et al.	324	158 R	4/25/1991
		5,258,985	11/2/1993	Spence, et al.	371	22.4	11/12/1991
		5,260,949	11/9/1993	Hashizume, et al.	371	22.3	12/14/1990
		5,276,807	1/1/1994	Kodoma, et al.	395	309	4/13/1987
		5,278,494	1/11/1994	Obigane	324	158 F	2/19/1992
		5,279,975	1/18/1994	Devereaux, et al.	437	8	2/7/1992
		5,286,656	2/15/1994	Keown, et al.	437	7	11/2/1992
		5,291,025	3/1/1994	Smith	250	561	11/30/1992
		5,297,277	3/22/1994	Dein, et al.	395	575	8/31/1990
		5,303,148	4/12/1994	Mattson, et al.	364	413.01	11/27/1987
		5,313,158	5/17/1994	Joosten, et al.	324	158 R	1/12/1993
		5,315,241	5/24/1994	Ewers	324	158 R	9/18/1991
		5,317,205	5/31/1994	Sato	307	443	6/2/1992
		5,319,754	6/1/1994	Meinecke, et al.	395	325	10/3/1991
		5,321,322	6/14/1994	Verheyen, et al.	307	465.1	3/24/1993
		5,329,471	7/12/1994	Swoboda, et al.	364	578	6/2/1987
		5,334,857	8/2/1994	Mennitt, et al.	257	48	4/6/1992
		5,343,478	8/1/1994	James, et al.	371	22.3	11/27/1991
		5,353,308	10/4/1994	Whetsel	371	22.3	8/6/1990
		5,355,369	10/11/1994	Greenberger, et al.	371	22.3	4/26/1991
		5,366,906	11/22/1994	Wojnarowski, et al.	437	8	10/16/1992
		5,371,390	12/6/1994	Mohsen	257	209	11/4/1992
		5,377,198	12/27/1994	Simpson, et al.	371	22.3	11/27/1991
		5,388,216	2/1/1995	Oh	395	849	10/3/1991
		5,389,556	2/14/1995	Rostoker, et al.	437	8	7/2/1992
		5,389,873	2/14/1995	Ishii, et al.	324	158.1	5/18/1993

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		5,390,131	2/14/1995	Rohrbaugh, et al.	364	490	4/6/1992
		5,391,984	2/14/1995	Worley	324	158.1	11/1/1991
		5,396,170	3/7/1995	D'Souza, et al.	324	158.1	4/25/1991
		5,399,505	3/21/1995	Dasse, et al.	437	8	7/23/1993
		5,420,874	5/30/1995	Kromer	371	47.1	4/20/1993
		5,424,651	6/13/1995	Green, et al.	324	754	3/27/1992
		5,426,650	6/20/1995	Ganapathy, et al.	371	22.3	11/24/1992
		5,428,622	6/27/1995	Kuban et al.	371	22.3	3/5/1993
		5,430,735	7/4/1995	Sauerwald, et al.	371	22.3	10/10/1989
		5,434,804	7/18/1995	Bock, et al.	364	579	12/29/1993
		5,442,282	8/15/1995	Rostoker, et al.	324	158.1	7/2/1992
		5,446,395	8/29/1995	Goto	324	763	9/21/1993
		5,448,576	9/5/1995	Russell	371	22.3	10/29/1992
		5,450,415	9/12/1995	Kamada	371	22.3	11/19/1993
		5,453,992	9/26/1995	Whetsel	371	22.3	8/2/1993
		5,457,400	10/10/1995	Ahmad, et al.	324	763	4/10/1992
		5,469,473	11/21/1995	McClear, et al.	375	219	4/15/1994
		5,471,481	11/28/1995	Okumoto, et al.	371	22.3	5/17/1993
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